

7/78
ELECTRONICS

up-to-date electronics for lab and leisure

July/August 1977
double issue-90p

with more than
100 circuits



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summer circuits : 100+ !

More than 100 circuits in one issue.

Complete units, extension circuits, design ideas, tips.

The recipe is quite simple:

Dream up wild ideas — some of them really wild! — and incorporate them in practical circuits.

Cull some novel ideas from stacks of manufacturer's application notes — and then test them to make sure they really work . . .

Evaluate hundreds of reader's contributions, select the most interesting ones — and test and (where necessary) improve them.

Squeeze 'more than 100' of these circuit ideas into a manageable number of pages.

The result is our traditional July/August double issue.

For those readers of this issue who don't (yet) know Elektor, it should be stressed that this is *not* a 'normal' issue. We only do this sort of thing once a year! Nor is this issue a review of circuits already published, nor is it a preview of circuits that will be discussed in greater detail in the coming year.

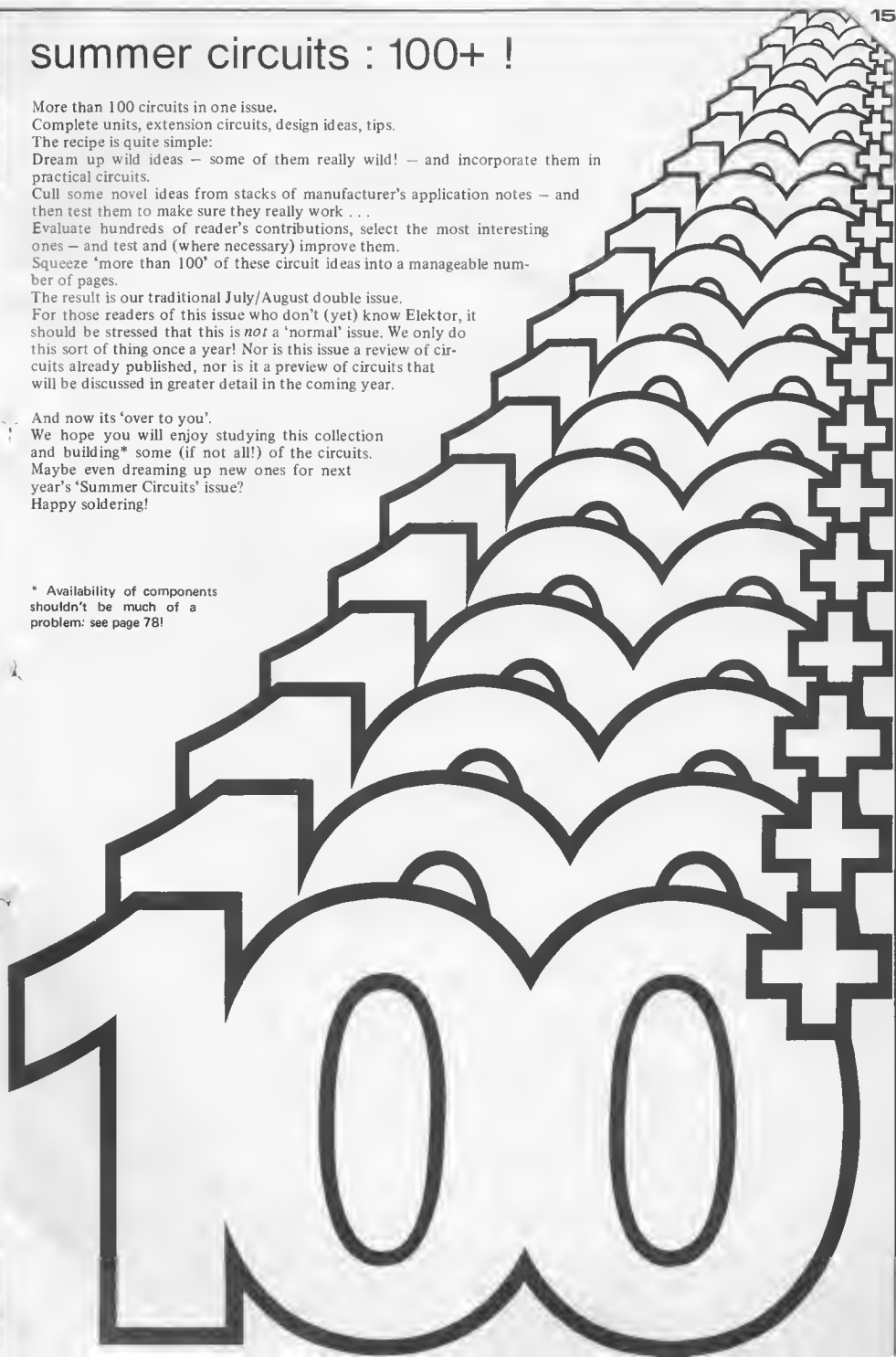
And now it's 'over to you'.

We hope you will enjoy studying this collection and building* some (if not all!) of the circuits.

Maybe even dreaming up new ones for next year's 'Summer Circuits' issue?

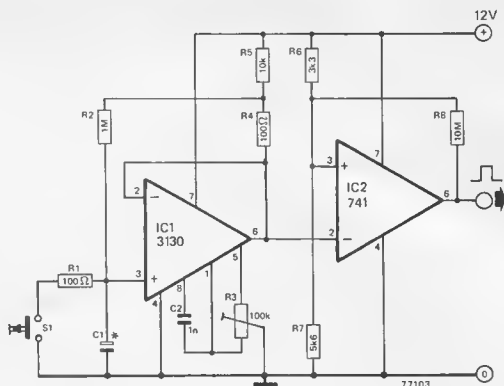
Happy soldering!

* Availability of components shouldn't be much of a problem: see page 78!





long interval timer



*see text

The drawback of most analogue timers (monostable circuits) is that, in order to obtain reasonably long intervals, the RC time constant must be correspondingly large. This invariably means resistor values in excess of 1 M Ω , which can give timing errors due to stray leakage resistance in the circuit, or large electrolytic capacitors, which again can introduce timing errors due to their leakage resistance.

The circuit given here achieves timing intervals up to 100 times longer than those obtainable with standard circuits. It does this by reducing the charging current of the capacitor by a factor of 100, thus increasing the charging time, without the need for high value charging resistors.

The circuit operates as follows: when the start/reset button is pressed C1 is discharged and the output of IC1, which is connected as a voltage follower, is at zero volts. The inverting input of comparator IC2 is at a lower potential than the non-inverting input, so the output of IC2 goes high.

The voltage across R4 is approximately 120 mV, so C1 charges through R2 at a current of around 120 nA, which is 100 times lower than could be achieved if R2 were connected direct to positive supply.

Of course, if C1 were charged from a constant 120 mV it would quickly reach this voltage and would cease to charge. However, the bottom end of R4 is returned to the output of IC1, and as the voltage across C1 rises so does the output voltage and hence the charging voltage applied to R2.

When the output voltage has risen to about 7.5 volts it will exceed the voltage set on the non-inverting input of IC2 by R6 and R7, and the output of IC2 will go low. A small amount of positive feedback provided by R8 prevents any noise present on the output of IC1 from being amplified by IC2 as it passes through the trigger point, as this could otherwise give rise to spurious output pulses.

The timing interval is given by the equation:

$$T = R_2 C_1 \left(1 + \frac{R_5 + R_6}{R_4} \right) \ln \left(1 + \frac{R_7}{R_6} \right)$$

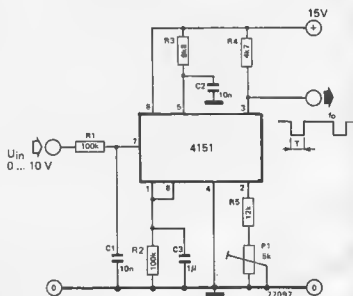
This may seem a little complicated, but with the component values given the interval is 100 \times C1, where C1 is in microfarads, e.g. if C1 is 1 μ the interval is 100 seconds. It is evident from the equation that the timing interval can be varied linearly by replacing R2 with a 1 M Ω potentiometer, or logarithmically by replacing R6 and R7 with, say, a 10 k Ω potentiometer.



voltage-frequency converter

Using only a few components and an integrated switching circuit it is possible to construct a high-performance voltage-frequency converter. With the component values shown in the diagram, the conversion ratio has a linearity of approx. 1%. An input voltage from 0 V ... 10 V will produce a corresponding 0 ... 10 kHz squarewave output voltage. By means of potentiometer P1, the circuit can be adjusted so that an input voltage of 0 V will produce an output frequency of 0 Hz.

The components which determine the frequency are resistors R2, R3, R5, P1 and capacitor C2. Using the formulae shown in the diagram, the conversion ratio of the circuit can be altered so that the circuit can be used for a number of different applications. When calculating the product of $T = 1.1 R_3 C_2$ care should be taken to ensure that this is always less than half the minimum output period, i.e. the positive output pulse should always be at least as long as the negative pulse.



$$f_{\text{out}} = \frac{0.486 \cdot (R_5 + P_1)}{R_2 \cdot R_3 \cdot C_2} \left[\frac{\text{kHz}}{\text{V}} \right]$$

$$T = 1.1 \cdot R_3 \cdot C_2$$

3

capacitance-frequency converter

G. Geiger

This simple circuit will produce a pulse train whose (average) frequency is directly proportional to the value of a capacitor which is to be tested. This waveform can thus be fed direct to a frequency counter which will then indicate the capacitance value in (tens of) picofarads.

The circuit is based on a monostable multivibrator whose pulse width is given by:

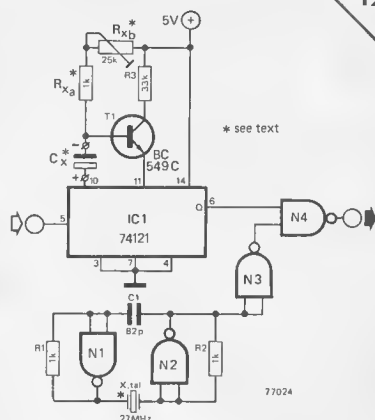
$$t = C_X \cdot R_X \cdot \ln 2.$$

If R_X is fixed then t is obviously proportional to C_X .

The output pulse of the monostable is used to gate pulses from a stable oscillator through to the input of a frequency counter. The number of pulses allowed through to be counted is thus proportional to t which is proportional to C_X .

The reference oscillator uses a normal 27 MHz (model control band) third overtone crystal, but in this circuit it oscillates at its fundamental of around 9 MHz. The monostable IC1 is triggered by gate pulses from the frequency counter and allows pulses from the oscillator through N4 to the counter input. For the circuit to function correctly the counter gate period must be longer than the longest period of the monostable, which with the values shown is around 20 ms.

To calibrate the circuit a capacitor of accurately known value is connected across the C_X terminals and the preset is adjusted until the count indicated is equal to the capacitance value in tens of picofarads, e.g. a 10 nF capacitor should give a count of 1000 (not 10000!). Any 1% silver mica capacitor



N1...N4=IC 2=7400

of greater than 1000 pF can be used for this purpose. In order that the calibration of the circuit should not be affected by temperature R_{XB} should be a good-quality multi-turn cermet trimmer.

With the values shown the circuit will measure capacitance values from 1000 pF to 1 μ F. The range may be extended to include higher values by reducing the value of R_X .

4

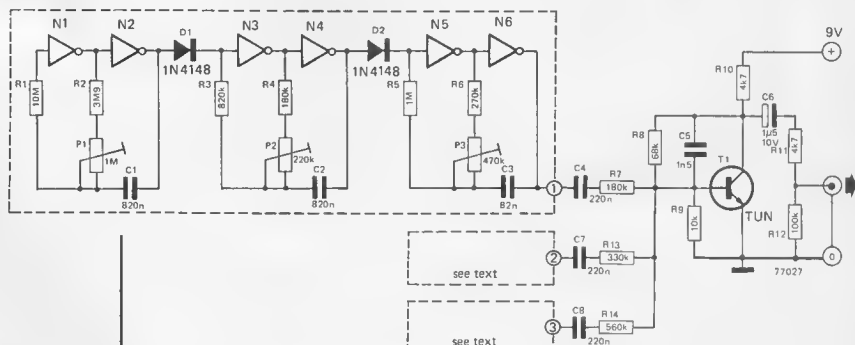
electronic scarecrow

This circuit produces a good imitation of machine-gun fire, an effect which should be sufficient to deter the most persistent of birds.

The system consists of three squarewave oscillators using CMOS inverters, all running at different frequencies. Oscillator N1/N2

speaker.

The circuit can also be used to produce background noises for devotees of war games. For this purpose a mixing amplifier stage, T1, may be provided, and inputs from several different oscillators combined. The use of different values for the mixer input



IC1=N1...N6=4049

gates oscillator N3/N4, which in turn gates oscillator N5/N6. The result is that this last oscillator produces intermittent bursts of pulses, which makes the sound very realistic. The output can be taken from the right-hand side of C4 and be fed to an audio amplifier and suitable (weatherproof) loud-

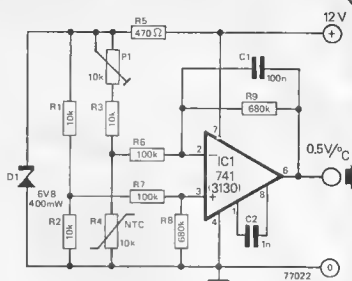
speakers R7, R13 and R14 means that the input signals will be amplified by different amounts, thus producing a more varied sound. P1, P2 and P3 can be adjusted experimentally to give the most pleasing results.

5

temperature-to-voltage converter

This circuit provides a simple means of constructing an electronic thermometer that will operate over the range 0 to 24°C (32 to 75°F). The circuit produces an output of approximately 500 mV/°C, which can be read off on a voltmeter suitably calibrated in degrees.

In order that the circuit should be kept simple the temperature sensing element is a negative temperature coefficient thermistor (NTC). This has the advantage that the temperature coefficient of resistance is fairly large, but unfortunately it has the disadvantage that the temperature coefficient is not constant and the temperature-voltage output of the circuit is thus non-linear. However, over the range 0 to 24°C the linearity is sufficiently good for a simple thermometer. Op-amp IC1 is connected as a differential amplifier whose inputs are fed from a bridge circuit consisting of R1 to R4. R1, R2, R3 and P1 form the fixed arms of the bridge, while R4 forms the variable arm. The voltage at the junction of R1 and R2 is about 3.4 volts. With the NTC at 0°C P1 is adjusted so that the output from the op-amp is zero, when the voltage at the junction of R3 and R4 will also be 3.4 V. With increasing temperature the resistance of the NTC decreases and the voltage across it falls, so the output of the op-amp increases. If the output is not exactly 0.5 V/°C then the values of R8 and R9 may be increased or



decreased accordingly, but they should both be the same value.

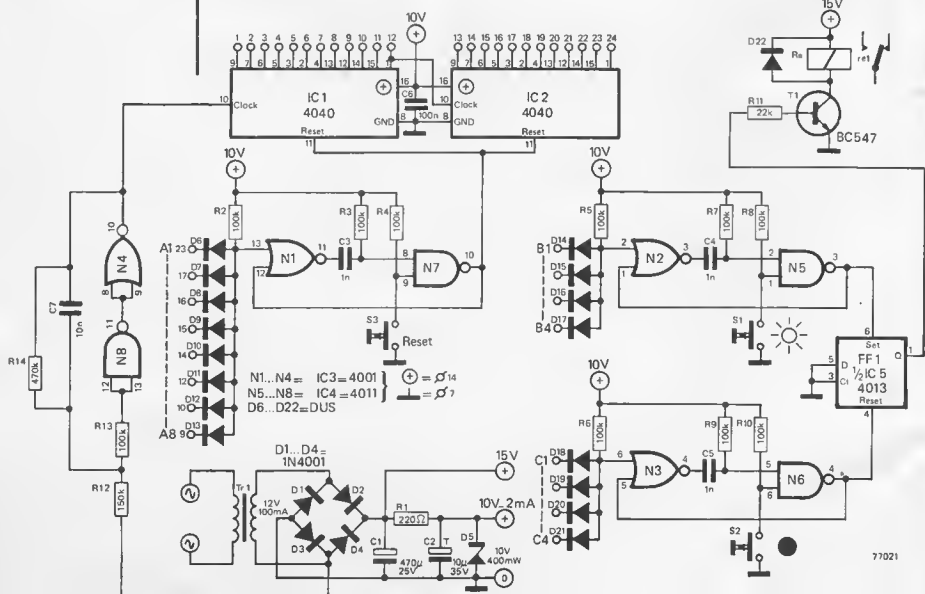
The IC can be a general purpose op-amp such as a 741, 3130 or 3140. The compensation capacitor C2 is not required if a 741 is used since this IC is internally compensated. Almost any 10k NTC thermistor may be used for R4, but the smaller types will obviously give a faster response since they have a lower thermal inertia. 5k or 15k types could also be used, but the values of P1 and R3 would have to be altered in proportion.

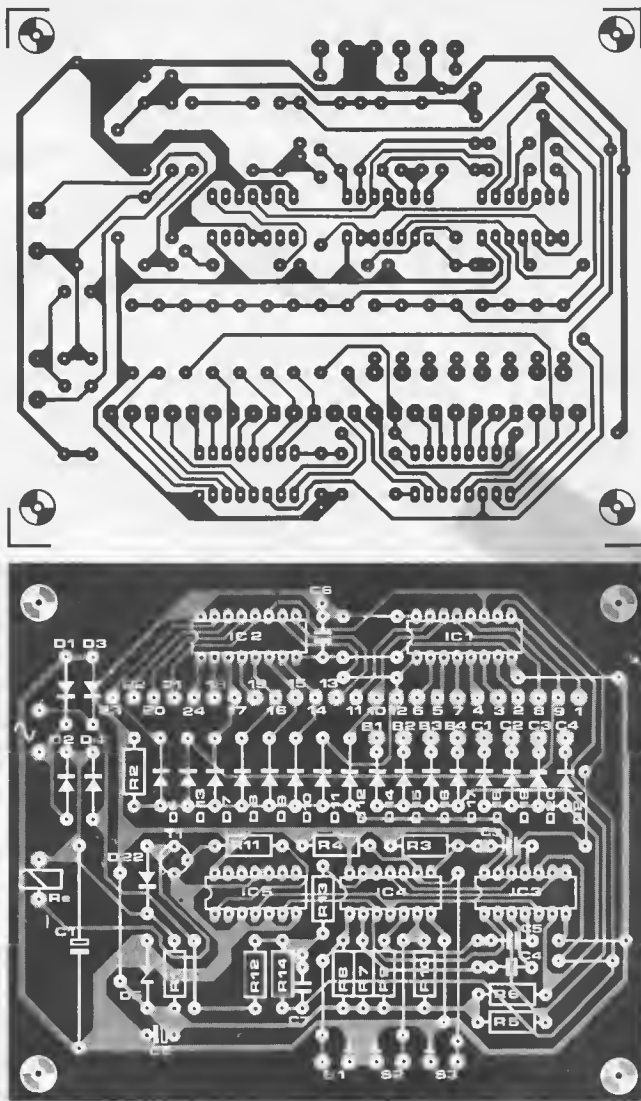
6

multi-purpose time switch

Using two CMOS counters it is a simple matter to construct a versatile time switch. The total cycle time of the switch can be set between zero and 93.2 hours, and the time switch can be made to switch equipment on and off at any time during this cycle. The reference frequency for the timer is the 50 Hz mains frequency. Two 4040 counters are connected in cascade and count the 50 Hz pulses. Each of these ICs is a 12-bit counter, so the maximum time that the counters will count to is 0.02×2^{24} seconds, where 0.02 seconds is the period of the mains waveform. This is equal to 93.206

hours. If a shorter cycle time is required it is necessary that the counters be reset when the required count is reached. As an example suppose that the desired cycle time is 24 hours. The counter must therefore count up to $24 \times 60 \times 60 \times 50 = 432000$, which in binary is 1000001111010100000000. Where a 1 occurs in this number the corresponding counter output is connected to one of the inputs of the diode AND gate D6 to D13. When the desired count is reached these outputs will all be high simultaneously and monostable N1/N7 will be triggered, giving





the counter a reset pulse.

A manual reset button is also provided. Any other desired cycle time up to the previously mentioned maximum may also be accommodated, but obviously some counts will require more or less diodes in the AND gate. The switch-on and switch-off times of the equipment to be controlled are also determined in the same manner. The binary equivalents of the on and off times are calculated and the appropriate counter outputs are connected to AND gate inputs B1 to B4 for switch-on and C1 to C4 for switch-off. At switch-on monostable N2/N5 is triggered, which sets flip-flop FF1, turning on T1 to activate the relay. At switch-off monostable N3/N6 is triggered, which resets FF1. Manual controls are also provided. If several circuits are to be controlled with

different switch-on and switch-off times then N2, N3, N5, N6, FF1 and T1 may be duplicated.

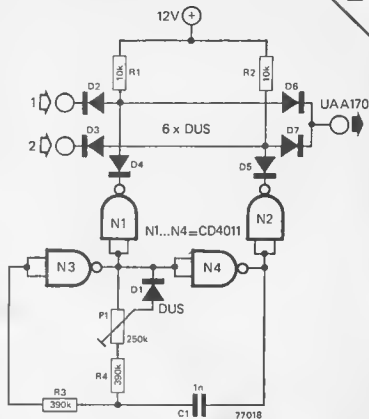
The one disadvantage of this circuit is that initially it must be reset at the time that the timing cycle is required to start, i.e. there is no time-setting facility, so in the event of a power failure it would be necessary to wait until the correct start time before resetting the circuit. For this reason it is best to make the start of the timing sequence occur at a convenient moment, such as in the morning or early evening.

To make the clock input of the counter less susceptible to interference pulses on the mains waveform it may be a good idea to precede it by a Schmitt-trigger using two CMOS NAND gates as described elsewhere in this issue.

UAA170 economiser

The Siemens UAA170, which has frequently been featured in this magazine, is an LED voltmeter which will light one LED in a column of sixteen according to the input voltage. The object of the circuit described here is to obtain the maximum use from a single UAA170 IC in applications where the full sixteen LED resolution is not required. For example, if a column of eight LEDs will suffice then a single UAA170 can be made to drive two such columns in response to two independent input voltages. LEDs 1 to 8 connected to the UAA170 outputs form one display channel, and LEDs 9 to 16 form the other channel.

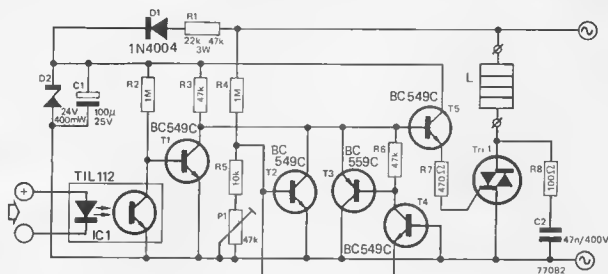
The two input voltages are switched alternately to the UAA170 input by an electronic switch analogous to an oscilloscope beam-switch. This consists of an astable multivibrator and two inverting buffers driving two diode switches. When the output of N1 is high the voltage on input 1 is allowed to pass to the output, but the output of N2 is low and the anodes of D3 and D7 are held to about 0.6 V by D5, so no voltage from input 2 appears at the output. When the output of N2 is high the reverse occurs. For the circuit to work the two input voltages must never overlap; e.g. if input 1, which causes LEDs 1 to 8 to light, has a range from 0 to 5 V, then input 2 must have a range from 5 to 10 V. This is easily accomplished by feeding the voltage to input 2 through the level shifter described elsewhere in this issue. The only other constraint is that the input 2 voltage should not exceed about 11.4 V at any time as this is the maximum



that can be handled by the channel switch. The input impedance of each channel is 10 k, determined by R1 and R2, and if a higher input impedance is required then buffer stages must be used.

P1 adjusts the duty-cycle of the astable multivibrator and hence the relative brightness of the two sets of LEDs. In some cases it may be necessary to reverse D1 to obtain the range of adjustment required to make the brightness equal.

triac relay



It is well-known that, for minimum generation of interference pulses, triacs should be triggered near the zero-crossing point of the mains waveform. There are a number of zero-voltage switch ICs in existence, but unfortunately these are expensive and often difficult to obtain.

As these ICs need a number of external components in order to function, a discrete component version of the circuit need not take up much more space, and is certainly cheaper.

The mains input is rectified by D1, dropped by R1 and stabilised by D2 to provide a 24 V DC supply. The control input is connected via an opto-isolator to isolate the control circuits from the mains. When no control voltage is applied the LED is not lit, the phototransistor is turned off and T1 is turned on. T5 is thus turned off and the triac cannot fire. When a control signal is present the LED is lit and T1 is turned off. The voltage comparator comprising T2 to T4 now compares a portion of the mains waveform from the potential divider R4, R5, P1 with the zero volt reference at the base of T4. As the mains waveform crosses zero the com-

parator turns on T5, which fires the triac. The duration of the trigger pulse can be varied up to a maximum of 1.5 ms by P1 (750 μ s each side of zero-crossing) and it is essential that by the end of this time the current taken by the load is greater than the holding current of the triac, otherwise the triac may turn off when the trigger pulse ceases. This places a constraint on the minimum load current that the circuit will switch, which depends on the holding current of the triac used. The maximum load current is determined by the maximum current rating of the triac.

With R1 = 47 k, when the circuit triggers the 24 V supply will drop to between 10 and 20 V, depending on the width of the trigger pulse, and the triac gate current will be between 18 and 40 mA. This may be increased by reducing the value of R1. As R1 has virtually the full mains voltage across it, for safety and reliability it is best to make up R1 from two series resistors, and to make the wattage rating fairly generous. Even with R1 = 22 k the dissipation in R1 is only one watt, but nevertheless it is rated at 3 W for reliability.

11

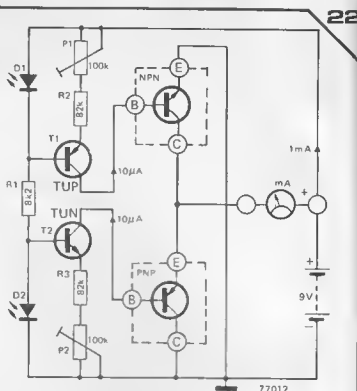
simple transistor tester

This simple circuit checks the functioning and measures the current gain (h_{FE}) of PNP or NPN bipolar transistors. It operates by feeding a known constant current into the base of the transistor and measuring the collector current. Since the collector current of a non-saturated transistor is h_{FE} times the base current (which is known) it is a simple matter to calculate the value of h_{FE} , and in fact the meter which measures the collector current can be calibrated directly in h_{FE} .

Since both PNP and NPN transistors must be tested, two constant current sources are required, to provide a negative base current for PNP transistors and a positive base current for NPN transistors. The voltage dropped across the LED causes a constant current to flow through the emitter resistor of the TUP and a corresponding constant collector current, which flows into the base of the NPN transistor under test. This current can be set to 10 μA by connecting a 50 μA meter between points B and E and adjusting P1.

The lower LED and TUN constitute the negative current source. Here again, this may be set to $10\mu\text{A}$ by connecting a microammeter between the lower points B and E, and adjusting P2.

When a transistor is plugged into the appropriate socket a current of $10\mu\text{A}$ will thus flow into the base and a current of h_{FE} times this will flow through the milliammeter. The full-scale deflection of the milliammeter depends on the maximum h_{FE} to be measured. Since the collector current is h_{FE} times the base current (which is $.01\text{ mA}$) a reading of 1 mA corresponds to an h_{FE} of 100, so if a 5 mA meter is to hand it can be calibrated in h_{FE} values from 0 to



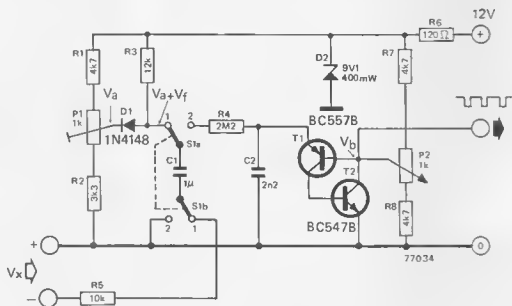
500, which should be adequate for most run-of-the-mill transistors. However, for testing 'C' versions of small-signal transistors, which can have gains up to 800, a 10 mA meter calibrated 0 to 1000 could be used, or a lower f.s.d. meter shunted to read 8 mA and calibrated 0 to 800.

Readers may have noticed that it is actually the emitter current of the PNP transistor that is measured, which is of course $1 + \beta_{FE}$ times the base current. However, since few transistors have gains less than 50 the worst error introduced by this is less than 2%, which is probably less than the error of the milliammeter.

Note. The use of LEDs as reference diodes for constant current sources is dealt with elsewhere in this issue.

12

A/D
converter



This circuit will deliver a number of pulses which is directly proportional to a negative input voltage. The conversion takes place in two stages. With S1 in position 1 capacitor C1 will charge until the voltage across it is $V_a + V_f + V_x$, where V_a is the voltage at the slider of P1, V_f is the forward voltage of D1 and V_x is the (negative) input voltage. S1 is then switched to position 2, when this voltage will appear on the left-hand side of R4. C2 will charge from C1 through R4 until the emitter voltage of T1 equals $V_b + V_{be}$ T1, when T1 will conduct. Since T1 and T2 are connected in the familiar thyristor tetrode configuration T1 and T2 both turn hard on and C2 discharges rapidly to V_{be} T1. C2 will then recharge from C1 until T1 again conducts. Each time C2 is charged C1 loses a charge ΔQ equal to V_b C2.

This cycle repeats until the voltage on C1 has fallen below $V_b + V_{beT1}$, when T1 will no longer conduct. If P1 and P2 are adjusted

so that $V_a + V_f = V_b + V_{beT1}$ then this obviously occurs when the voltage on C1 has fallen to $V_a + V_f$, i.e. the portion of the voltage on C1 due to the input voltage V_X has been dissipated. The number of pulses appearing at the collector of T2 is thus proportional to this input voltage. Since C1 loses a charge ΔQ for each pulse the total number of pulses is obviously given by

$$N = \frac{Q_x}{\Delta O}, \text{ where } Q_x \text{ is the charge on Cl due to}$$

 V_x , which is $C1V_x$.

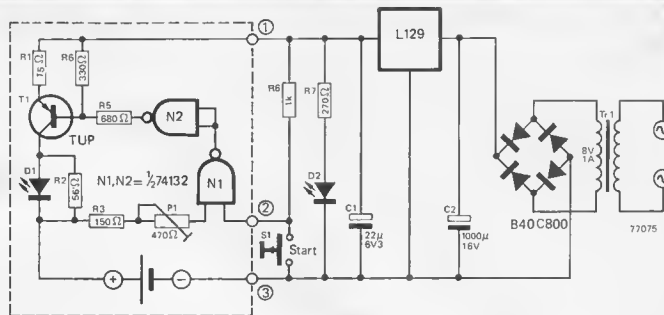
$$\text{Thus } N = \frac{C_1}{C_2 V_b} \times V_x$$

With the component values given the conversion factor is about 100 pulses per volt.

Source: Electronic Engineering, September 1976.

automatic NiCad charger

H. Knote



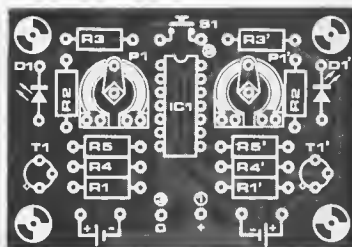
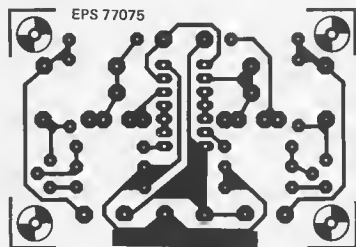
It is not generally appreciated that, if Nickel-Cadmium batteries are subjected to prolonged overcharging from chargers of the constant current type, their life may be considerably reduced. The charger described here overcomes this problem by charging at a constant current but switching off the charger when the terminal voltage of the battery rises, which indicates a fully-charged condition. The basic circuit described is intended to charge a single 500 mAh 'AA' cell at the recommended charge rate of around 50 mA, but it can easily be extended at little cost to charge more than one cell.

Power for the circuit is provided by a transformer, bridge rectifier and 5 V IC regulator. The cell is charged by a constant current source T1 which is controlled by a voltage comparator based on a TTL Schmitt trigger N1. While the cell is charging the terminal voltage remains at around 1.25 V, which is below the positive trigger threshold of N1. The output of N1 is thus high, the output of N2 is low and T1 receives a base bias voltage from the potential divider R4/R5. While the cell is being charged D1 is lit. When the cell approaches the fully-charged

state the terminal voltage rises to about 1.45 V, the positive trigger threshold of N1 is exceeded and the output of N2 goes high, turning off T1. The cell ceases to charge and D1 is extinguished.

As the positive trigger threshold of N1 is about 1.7 V and is subject to a certain tolerance, R3 and P1 are included to adjust it to 1.45 V. The negative trigger threshold of the Schmitt trigger is about 0.9 V, which is below the terminal voltage of even a fully-discharged cell, so connecting a discharged cell in circuit will not cause charging to begin automatically. For this reason a start button S1 is included which, when pressed, takes the input of N1 low.

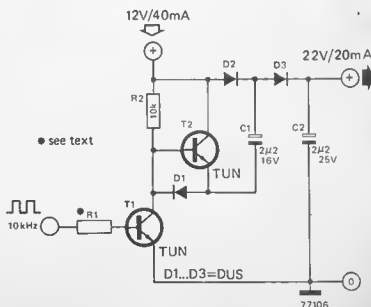
To charge a number of cells the portion of the circuit enclosed in the dotted box must be duplicated. This has the advantage that, unlike chargers in which cells are connected in series, cells in any state of discharge may be placed on the charger and each will be individually charged to the correct level. The disadvantage is that batteries of cells cannot be charged. However, up to ten AA cells may be charged if the circuit is duplicated the appropriate number of times.



two-TUN voltage doubler

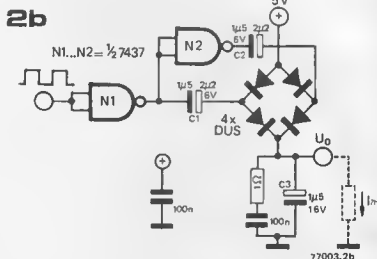
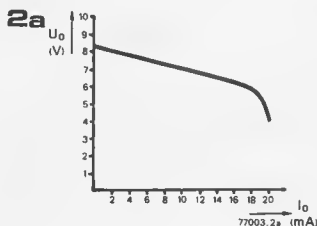
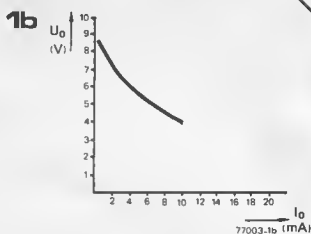
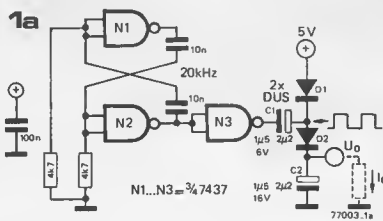
This little circuit will produce a DC output that is almost twice the supply voltage. A square-wave input is required of sufficient level to turn T1 fully on and off. When T1 is conducting, C2 is charged to just under the supply voltage. When T1 is cut off, T2 starts to conduct and raises the voltage at the negative end of C2 to just under the positive supply level. This implies that the voltage at the positive end of C2 is raised to almost twice the supply voltage, so that C3 will ultimately charge to this level. The circuit is remarkably efficient: the current drawn from the main supply is only marginally greater than twice the output current. In the example shown here, the efficiency is approximately 90%.

The value for R1 depends on the amplitude of the square-wave input: T1 will require a base current of 0.5 ... 1 mA. (RCA application note)



15

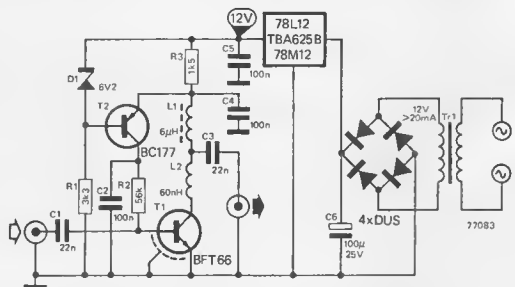
TTL voltage doubler



This voltage doubler can be used in circuits that have only a 5 V supply rail, where a higher voltage is required at a low current. Figure 1a shows the basic circuit, which uses three of the gates in a 7437 quad two-input NAND buffer IC. N1 and N2 are connected as a 20 kHz astable multivibrator, and the output of N2 drives N3, which acts as a buffer between the astable and the doubler circuit. When the output of N3 is low C1 charges through D1 and N3 to about +4.4 V. When the output of N3 goes high the voltage on the positive end of C1 is about 9 V, so C1 discharges through D2 into C2. If no current

is drawn from C2 it will eventually charge to about +8.5 V. However, if any significant current is drawn the output voltage will quickly fall, as shown in figure 1b. Much better regulation of the output voltage, as shown in figure 2a, can be obtained by using the push-pull circuit of figure 2b. This is driven from an identical astable to that in figure 1b. While the output of N1 is low and C1 is charging, the output of N2 is high and C2 is discharging into C3, and vice versa. Since C3 is being continually charged the regulation of the output voltage is much improved.

16

low-noise
V.H.F. aerial
amplifier

This simple aerial amplifier can be used to boost the level of weak FM signals. It has a gain of 22 dB, and the extremely low noise figure of 1.6 dB, so that it will not unduly degrade the signal-to-noise ratio. The amplifier consists of a single, low-noise BFT66 transistor T1 operating in common emitter configuration. Base bias is provided by a constant current source T2, which stabilises the operating point. The value of L1 is nominally 6 μ H, but any r.f. choke of a similar standard value (5.6 μ H or 6.8 μ H) may be used. L2 is a home-made coil consisting of five or six turns of 0.25 mm (33 SWG) enamelled copper wire. This is wound onto a 5 mm diameter former which is then removed and the self-supporting air-cored coil is stretched to about 10 mm length. When constructing the preamp care should be taken to keep all component leads as short as possible to avoid stray inductance

and capacitance. The circuit should be mounted in a screened metal box located as close as possible to the aerial. Use of an IC voltage regulator has the advantage of reliability and compactness. However, if such an IC is not readily obtainable, it may be replaced by a simpler circuit: a 680 Ω resistor between C5 and C6, and a 12 V/400 mW zener diode plus a 10 μ /16 V electrolytic capacitor in parallel with C5.

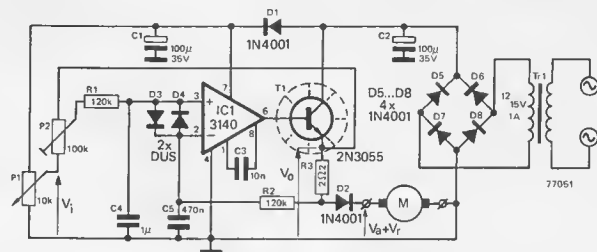
Specification

Frequency range:	1 MHz - 300 MHz.
Gain:	22 dB
Noise figure:	1.6 dB
Input and output impedance:	60 Ω
Supply voltage:	+12 V
Supply Current:	4 mA

Reference: Siemens Data on BFT66.

17

model speed control



The disadvantage of most simple speed controllers for model trains or cars is that they simply supply the motor with a fixed voltage. Consequently the speed does not remain constant, since the model slows down when climbing gradients and speeds up when going downhill. With model trains the setting of the control knob to maintain a particular speed also varies with the load that the engine is pulling.

The circuit described here eliminates this problem by monitoring the motor speed and keeping it constant for a given control setting, irrespective of load. The circuit will operate with most models which use a DC permanent magnet motor.

The terminal voltage of a motor consists of two components, the back e.m.f. generated by the motor and the voltage dropped across the armature resistance. The back e.m.f. is proportional to the motor speed and so motor speed can be sensed by measuring it, but the problem is to separate the back e.m.f. from the resistance voltage. If an external resistor is connected in series with the motor then, since the same current flows through it and through the armature resistance, the voltage drop across the series resistor will be proportional to the drop across the armature resistance. In fact if the two resistances are equal then the two voltages will be equal, and the voltage across the series resistor can be subtracted from the motor voltage, leaving only the back e.m.f. The circuit monitors the back e.m.f. and adjusts the motor current so that, for a given control setting, the back e.m.f., and hence the motor speed, remains constant.

To simplify the description of the circuit it

is assumed that P2 is set to its mid-position and that R3 is equal to the armature resistance of the motor.

The motor voltage is the sum of the back e.m.f. V_a and the voltage dropped across the internal resistance V_r . Since a voltage V_r is dropped across R3 the output voltage V_o equals $V_a + 2V_r$. The voltage at the inverting input of IC1 is $V_a + V_r$, and that at the non-inverting input is $V_i + \frac{V_a + 2V_r - V_i}{2}$.

These two voltages are equal,

$$\text{i.e. } V_a + V_r = V_i + \frac{(V_a + 2V_r - V_i)}{2}$$

Simplifying this equation gives $V_a = V_i$, which means that the back e.m.f. is always kept equal to the control voltage, so the motor runs at constant speed for a given setting of the speed control P1. P2 is used to compensate for the fact that R3 may not be equal to the armature resistance, by varying the amount of positive feedback to the non-inverting input.

To set up the circuit a model is run and P2 is adjusted until the speed just remains constant on gradients and with different loads. If P2 is turned too far towards P1 then the model will slow down, but if P2 is turned too far in the opposite direction then the model will actually go faster when climbing a gradient. If the controller is to be used with several different models then they must obviously all be fitted with similar motors, otherwise the circuit would require readjustment whenever a different model was used.

The output transistor T1 should be fitted with a heatsink of around 4°C/watt.

18

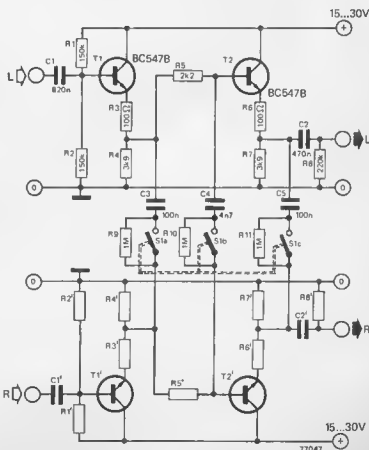
stereo noise filter

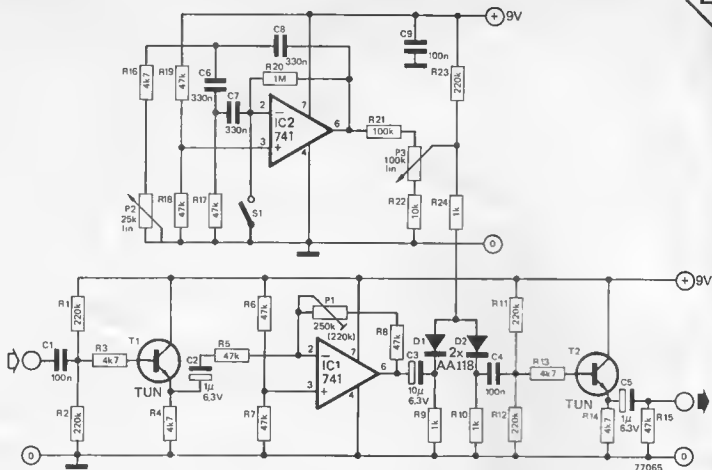
The signal-to-noise ratio of an FM broadcast received in stereo is considerably worse than that of the same broadcast received in mono. This is most noticeable on weak transmissions, when switching over from stereo to mono will considerably reduce the noise level. This noise reduction occurs because the left-channel noise is largely in anti-phase to the right-channel noise. Switching to mono sums the two channels and the anti-phase noise signals cancel.

By summing only the high-frequency components of the signal it is possible to eliminate the annoying high-frequency noise without destroying the stereo image since channel separation is still maintained at middle and low frequencies.

Each channel of the circuit consists of a pair of emitter followers in cascade, with highpass filters comprising R3 to R7 and C3 to C5 that allow crosstalk to occur between the two channels above about 8 kHz when switch S1 is closed. When S1 is open the two channels are isolated, but resistors R9 to R11 maintain a DC level on C3 to C5 so that switching clicks do not occur when S1 is closed.

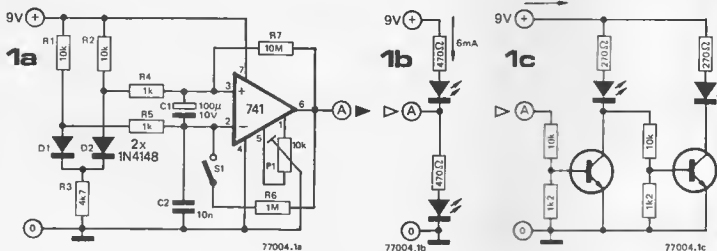
The stereo-mono crossover frequency can be increased by lowering the values of C3 to C5 or decreased by raising them.





Tremolo is one of the most popular effects used in electronic music. The tremolo effect is produced by amplitude modulating the music signal with a low-frequency signal of between 1 Hz and 10 Hz. The effect gives warmth and richness to the otherwise 'flat' sound of instruments such as electronic organs. The most pleasing effect is produced when the modulation waveform is sinusoidal. The music signal is buffered by emitter-follower T1 and is then fed into op-amp IC1, whose gain can be varied by means of P1.

The output of IC1 is fed to the diode modulator D1/D2, the output of which is buffered by a second emitter follower T2. The sinusoidal signal is generated by an oscillator built around IC2, whose frequency can be varied between 1 Hz and 10 Hz by P2. The output level, and hence the modulation depth, can be varied by P3. Switch S1, when closed, disables the oscillator, which allows the music signal to pass unmodulated.



This ingenious touch switch is operated, not by skin resistance or capacitance effects, but by heat. The circuit utilises the negative temperature coefficient of silicon diodes.

The 741 functions as a comparator with positive feedback and, for the purpose of describing the circuit it is assumed that the voltage drop across each diode is initially the same and that the op-amp output voltage is low. Due to the potentiometer effect of R4 and R5 the voltage on the non-inverting input of the op-amp will be pulled slightly lower than that on the inverting input.

If D1 is heated by touching it, its forward voltage drop will decrease, and so will the voltage on the inverting input of the op-amp. When this voltage falls below that on the non-inverting input the op-amp output will go high. Positive feedback via R5 and R4 will pull the non-inverting input still higher, so that even if D1 is subsequently allowed to cool to the same temperature as D2 the output will remain high.

The switch is returned to its original state by touching D2. This will cause the voltage at the non-inverting input to fall, and when it is

less than that on the inverting input the output of the op-amp will go low.

The output of the switch can be used to control other circuits, relays etc. To indicate the state of the switch two LEDs may be driven by the circuit. If a brighter display is required than can be driven direct from the op-amp output then a two transistor buffer may be used to drive LEDs at a higher current.

Before use the circuit must be nulled to compensate for differences in the diode forward voltage drops and for the offset voltage of the 741. This is done by closing switch S1, which inhibits the positive feedback loop, and by adjusting P1 until the op-amp output voltage is approximately half supply (4.5 V). The circuit may also be used as a differential thermostat in such applications as solar heating. In this case one diode is mounted on the solar panel and the other on the hot water tank. P1 is adjusted so that the circuit will operate when the required temperature difference between the two is reached. This is usually when the solar panel is 25 to 30°C hotter than the tank.

21

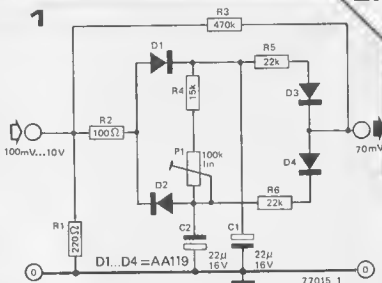
signal powered dynamic compressor

This dynamic range compressor will provide approximately 20 dB of compression over the input voltage range 100 mV to 10 V. An unusual feature of the circuit is that it requires no power supply, the control voltage for the voltage-controlled attenuator being derived from the input signal.

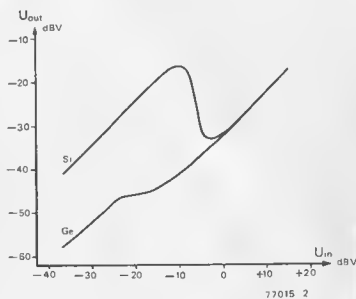
A portion of the input signal is rectified by D1 and D2 and used to charge capacitors C1 and C2. These provide a control voltage to the diode attenuator comprising R3, R5, R6, D3 and D4. The diodes operate on the non-linear portion of their forward conduction curve. At low input signal levels the output signal appears with little attenuation. As the signal level increases so does the rectified voltage on C1 and C2. The control current through the diodes increases and their dynamic resistance decreases, thus attenuating the output signal.

The attack time of the compressor is fixed and depends on the time constant consisting of C1 or C2, R2 and the output impedance of the circuit feeding the compressor, which should be as low as possible. The decay time of the compressor can be varied to a small extent by P1. The input impedance of the circuit that the compressor output feeds should be as high as possible.

The circuit works best with germanium diodes, since these have a low forward voltage threshold and a much smoother and more extended 'knee' than silicon types. The accompanying graph shows the response of the compressor using both silicon and germanium diodes, and it is obvious which are better!



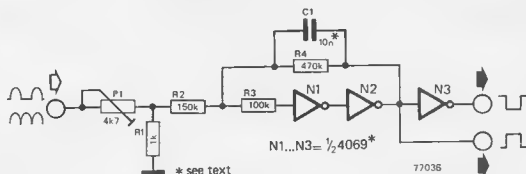
2



22

timebase input circuit

A.M. Bosschaert



Mains frequency is often used as a reference for digital clocks and other digital circuits. Unfortunately problems can arise if the 'raw' mains waveform is used without further processing, especially when driving clocks or other timing circuits, as mains transients can cause extra, unwanted counts to occur. The circuit described here will accept a half- or full-wave rectified mains input and provide a 50 or 100 Hz square-wave output, free from interference and suitable for driving CMOS or TTL logic circuits.

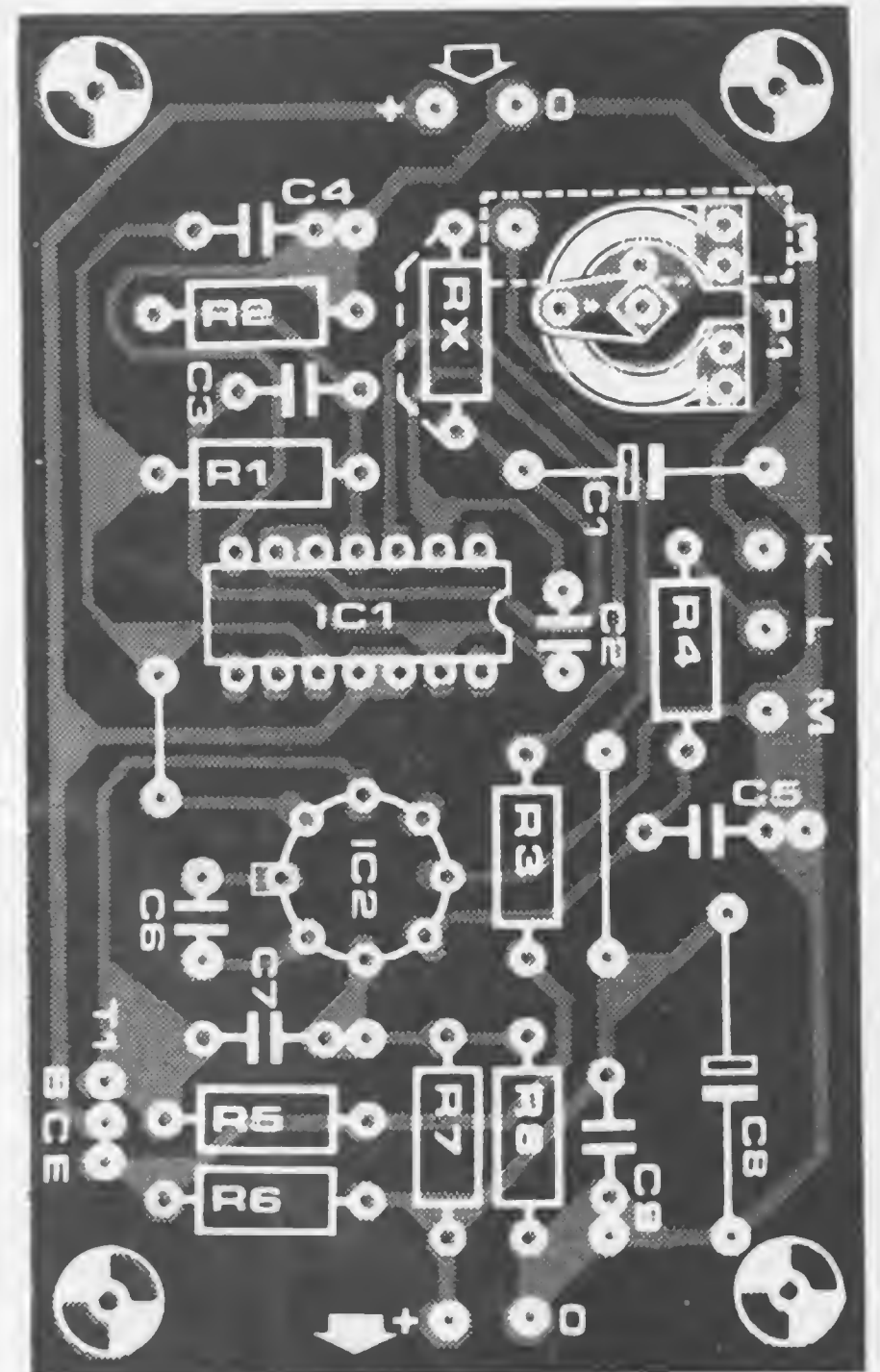
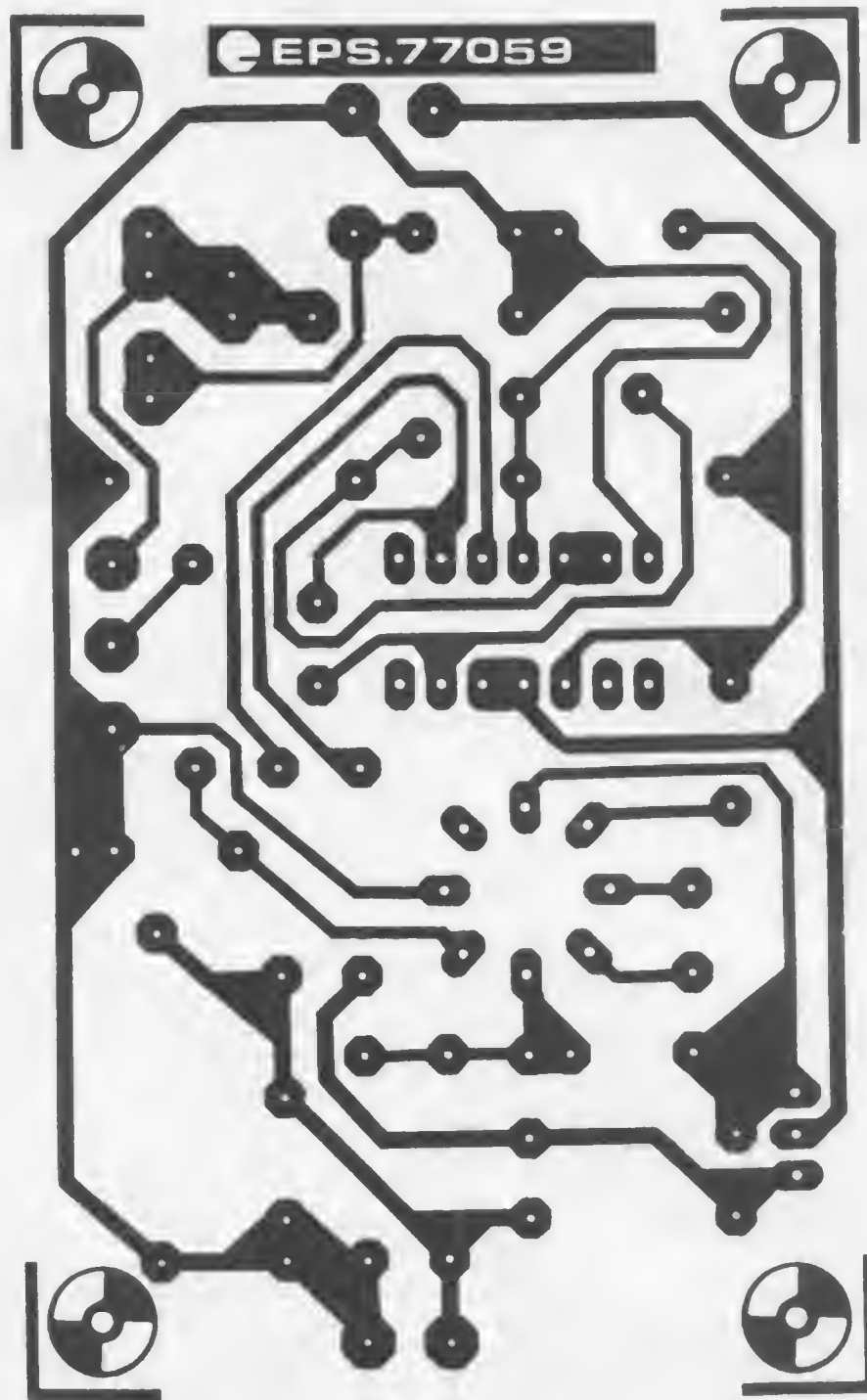
There are two methods of producing a clean squarewave from a noisy sinusoidal signal. The first approach is to use a Schmitt trigger with a large degree of hysteresis. Once the positive trigger threshold has been exceeded the output will go high and any small negative transients cannot then affect the output state until the input signal has fallen to near the negative trigger level. When the output has returned to the low state small positive transients cannot affect the output until the signal has again risen to near the positive trigger level.

The second approach is to use the input signal to trigger a monostable whose pulse length is just less than the period of the input signal. Once the monostable has been triggered any spurious pulses cannot affect the output state until the monostable resets, by which time the monostable is due to be triggered again anyway.

The circuit described here combines both these methods in a 'belt-and-braces' approach. The 50 Hz signal, taken from the

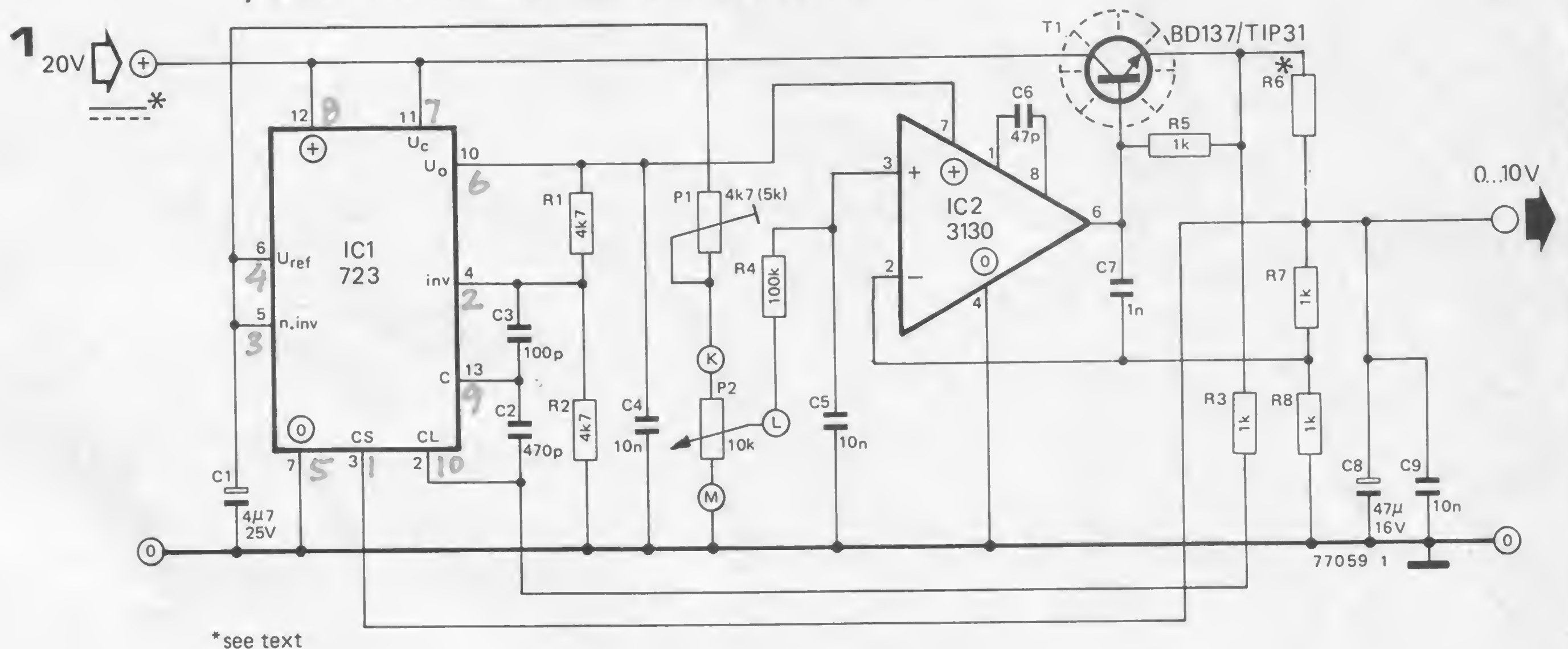
mains transformer secondary of the equipment, is either half-wave or full-wave rectified to give a 50 Hz or 100 Hz input signal. This is reduced to a level suitable for driving the circuit by a potential divider comprising P1 and R1. Two CMOS inverters N1 and N2 are cascaded with positive feedback from output to input via R4 to give a Schmitt trigger. The degree of hysteresis is determined by the ratio of R4 to R2. However, AC positive feedback is also provided via C1 so that, for a short time after the output of N2 has changed state, C1 will be charging or discharging and will present a low impedance across R4. This greatly increases the hysteresis and effectively causes the circuit to latch up so that it cannot be triggered by spurious pulses. A squarewave output is available at the output of N2 and an inverted version of this waveform is available at the output of N3.

To set up the circuit P1 is adjusted until the circuit triggers reliably. If possible P1 should be adjusted until the output is a square-wave with a 50% duty cycle. If the circuit is to be used to drive CMOS logic then either a 4049 or 4069 may be used for N1 to N3, and the supply voltage should be the same as that of the circuits which are being driven (+3 to +15 V). If TTL circuits are being driven then the supply voltage must obviously be the same as the TTL supply (+5 V) and a 4049 should be used for N1 to N3. For reliable triggering the peak value of the input signal should be equal to or greater than the supply voltage.

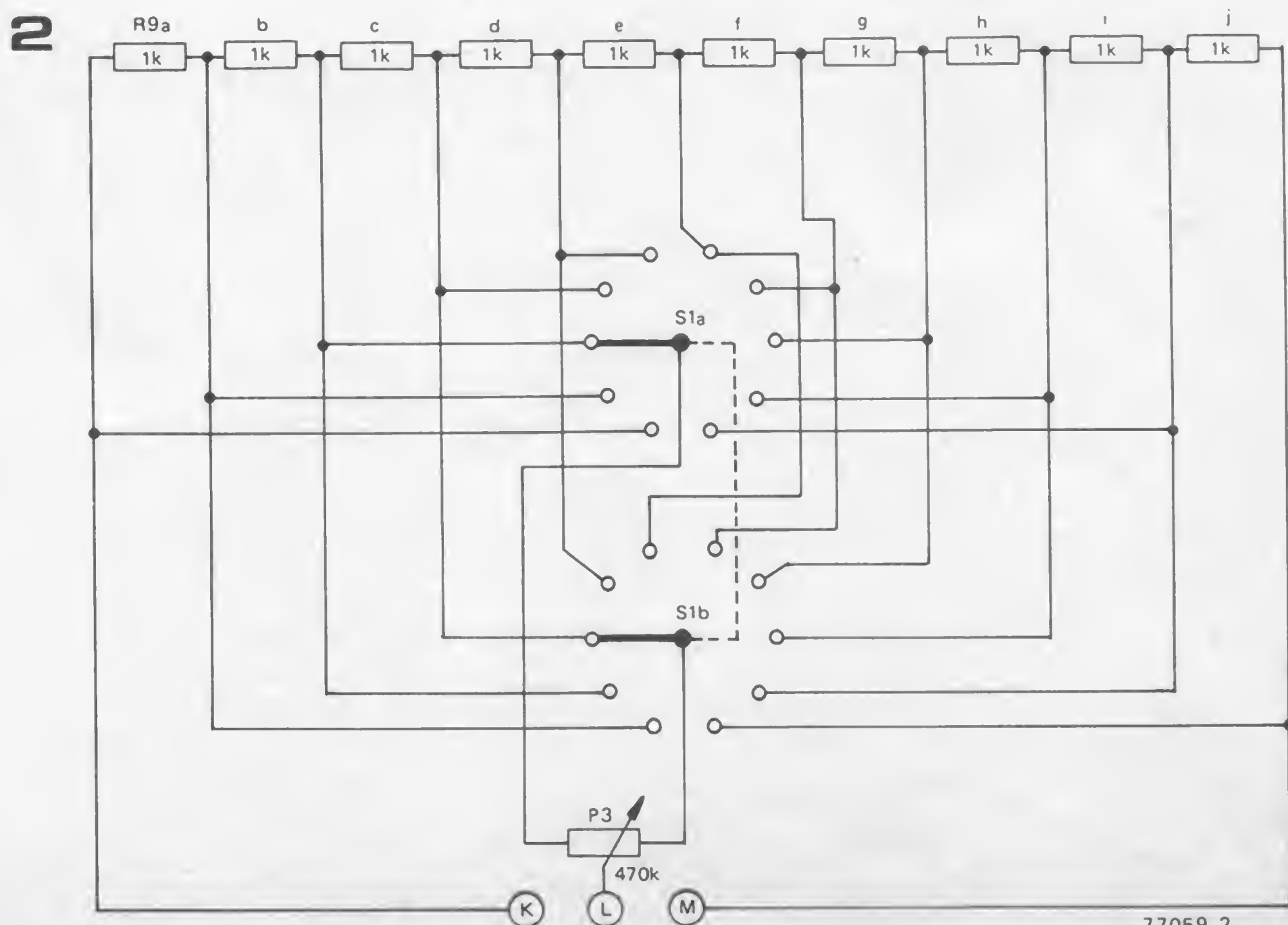


16 V transformer winding, bridge rectifier and 1000 μ F electrolytic capacitor. Initial calibration is quite straightforward. Set P1 to its maximum value (the slider turned down towards point K) and turn P2 all the way up (to point K). Now adjust P1 until the output voltage is exactly 10 V. P2 can be provided with a linear 0 ... 10 V scale. It is advisable to use a high-quality

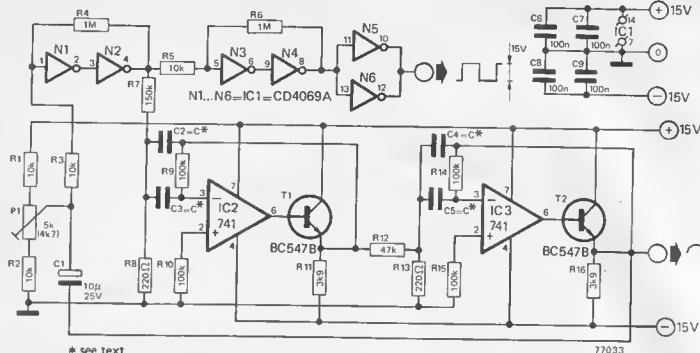
potentiometer here; a multiturn type will prove useful if precise and stable setting of the output voltage is required. Alternatively, the circuit shown in figure 2 can be used. In this case, the output voltage can be altered in 1 V steps by means of the 10-position switch, and P3 allows fine-adjustment within each 1 V step.



*see text



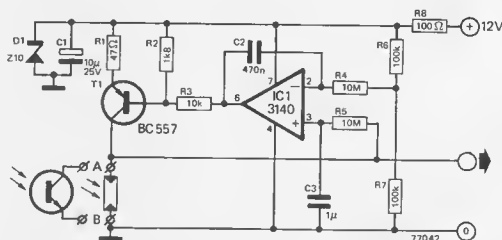
25

spot-frequency
sinewave
generator

This circuit employs an unusual method of producing a sinewave signal and, unlike most sinewave generators, requires no amplitude stabilising components such as thermistors or FETs. N1 and N2 are connected as a Schmitt trigger at whose output appears a squarewave (how this happens will become apparent). The squarewave signal is fed into two cascaded selective filters consisting of IC2/T1, IC3/T2 and their associated components. The filters remove the harmonic content of the squarewave leaving only the sinusoidal fundamental. This signal is fed back via C1 to the input of the Schmitt trigger. At each zero-crossing of the sinewave the Schmitt trigger changes state, thus producing the original squarewave that is fed to the input of IC2. P1 adjusts the

trigger point of the Schmitt trigger, which varies the duty-cycle of the squarewave and hence the sinewave purity. By suitable adjustment of P1 distortion levels of 0.15% to 0.2% can be achieved. With the ICs used lower figures are not possible due to the distortion introduced by IC3 and T2. N3 and N4 also function as a Schmitt trigger, which further speeds up the leading and trailing edges of the squarewave from N2. A squarewave signal with short rise and fall times, synchronised to the sinewave signal, is available at the outputs of N5 and N6. The value of C for a particular frequency f_0 is given by $C (\mu F) = \frac{0.34}{f_0 (\text{Hz})}$.

26

compensated
light sensor

Circuits which use photosensitive devices such as LDRs, photodiodes or phototransistors to sense rapid changes in light level (e.g. in optical tachometers) can be affected by changes in ambient light level altering the biasing of the photosensor. If the bias current is fixed this can lead to saturation of the photodevice at high ambient light levels.

This problem can be overcome by using a light-dependent current source that will alter the bias current to cope with changes in ambient light level and thus maintain a constant bias voltage across the photosensor. However, if the response time of the current source is made sufficiently long it will not respond to the rapid variations in light level such as those which the circuit is required to sense, and such variations will produce changes in output voltage. In addition, since the circuit is a current source it has an extremely high output impedance and thus does not load the photosensor output.

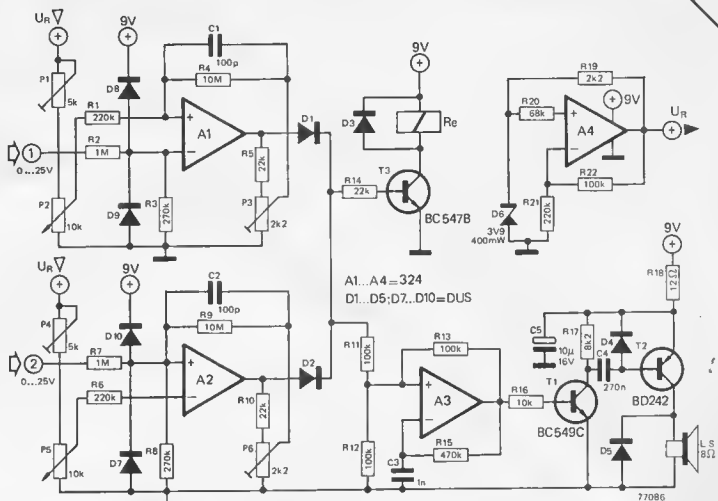
The circuit comprises a current source T1, which is driven by the output of op-amp IC1. The inverting input of IC1 is biased to about 5 V by R6 and R7 and feedback causes the output voltage of the IC to adjust itself until

the current supplied by T1 is such that the voltage dropped across the photosensor is equal to the voltage at the inverting input of the op-amp (about 5 V). This ensures that if the ambient light level (and hence the resistance of the photosensor) varies, the current through the photosensor will be adjusted to maintain a constant output voltage.

However, due to the time constants $R4 \cdot C2$ and $R5 \cdot C3$ the circuit cannot respond to variations in light level that occur at frequencies greater than about 2 Hz. The current source will thus 'ignore' these variations and will continue to supply a constant current, so that if the resistance of the photosensor varies due to rapid changes in light level the output voltage will vary in sympathy.

The circuit will function with a wide range of LDRs, phototransistors and photodiodes, the only constraint being that the resistance of the device connected between points A and B must not fall below 300 Ω . The total current consumption of the circuit is between 20 and 35 mA, depending on the current drawn by the photosensor.

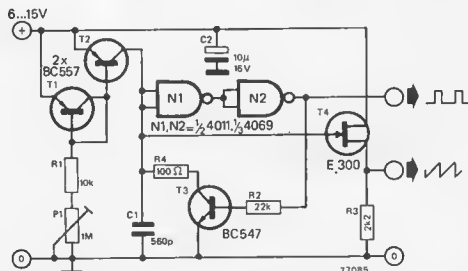
threshold box



The maximum input voltage to inputs 1 and 2 is 25 V and the input resistance is 1 M Ω , but the input voltage (and resistance) can be increased by raising the value of R2 and R7.

28

sawtooth-CCO



In place of NANDs inverters may be used.

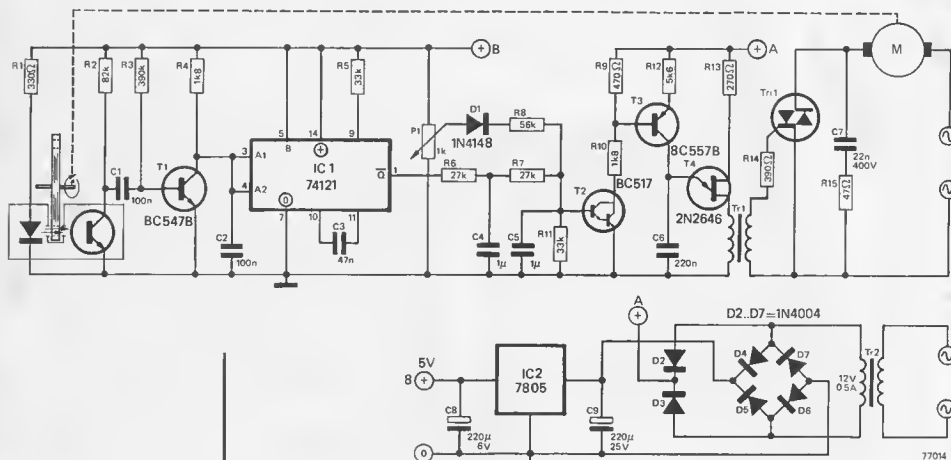
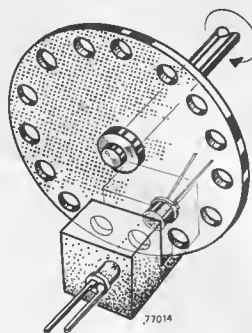
speed controller for motors

M. Junghans

Electric motors up to around a quarter horsepower can often be picked up very cheaply (ex-domestic appliances). They are extremely useful for driving bench saws, drilling machines etc. A speed controller that will set and maintain a near-constant speed under varying load conditions is a useful accessory in this type of application.

The motor speed is sensed by an optical commutator consisting of a disc with 15 holes or slots around its periphery. This interrupts a light beam falling on a photo-transistor, which turns T1 on and off. Pulses from the collector of T1 are used to trigger a monostable IC1 whose Q output is integrated by R6/C4 and R7/C5 to provide a DC output level which is inversely proportional to motor speed.

The desired motor speed is set by P1 and the



desired and actual motor speeds are compared by T2, T3 and T4 form a trigger pulse generator which produces a pulse to fire the triac once every half cycle of the mains waveform. T2 varies the collector current of T3 and hence the charging current of C6.

This in turn controls the point in the cycle at which the trigger pulse occurs.

If the motor speed should tend to rise then the voltage on C4 will fall and the base current of T2 will be reduced. The collector voltage of T2 will rise, thus reducing the current through T3, and the trigger pulse will occur later, causing the motor to slow down. If the motor tends to slow down the reverse will occur. The voltage on C4 will rise and the collector voltage of T2 will fall, thus increasing the collector current of T3 and causing the trigger pulse to occur earlier.

The trigger stage (T2...T4) is driven from an unsmoothed full-wave rectified supply (A). When T4 fires, it will discharge C6 rapidly and then remain conducting until the supply voltage approaches the next zero-crossing. The result is that C6 is always discharged at the start of each half-cycle, so the

position of the trigger pulses relative to the zero-crossings is determined solely by the current through T3. In other words, the trigger pulses are synchronised to the mains.

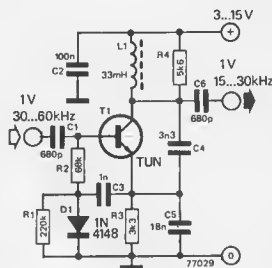
The type of triac required will obviously depend on the motor used. It should be rated for at least three times (!) the nominal mains voltage; the current will depend on the maximum motor current, and a reasonable rule-of-thumb is to divide the motor power rating by the mains voltage and multiply the result by two. As an example, a 500 W/245 V motor would require a triac rated at $\frac{500}{245} \times 2 \approx 4$ amps!

The trigger pulse transformer (Tr1) can be wound on a type AL250 potcore: primary 80 turns, secondary 40 turns, both 0.1 mm enamelled copper wire (42 S.W.G.).

Editorial note: In some cases it may be possible to dispense with the 'disc-with-holes'. If the LED and phototransistor are mounted inside the motor casing, the motor itself may sometimes be used to periodically interrupt (or reflect) the light beam.

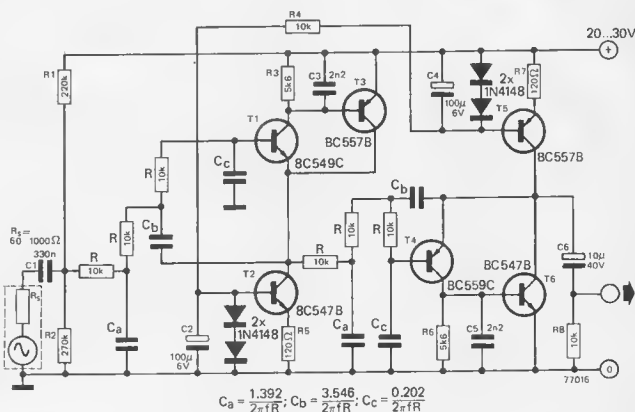
frequency divider using one TUN

A remarkable feature of the circuit is that amplitude modulation of the input signal by up to 70% will be reproduced at the output.



31

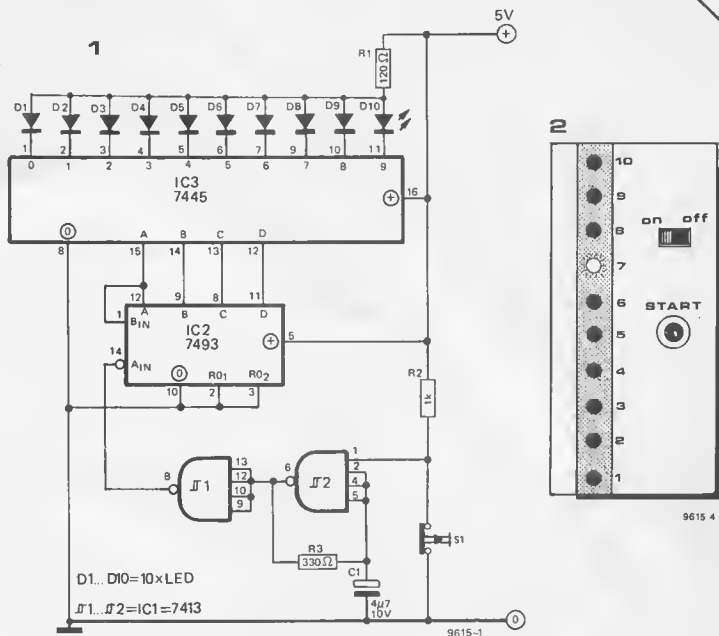
distortion
suppressor



The values of Ca, Cb and Cc for a 1 kHz cutoff frequency are 22 n, 56 n and 3n9 respectively. Other values can easily be calculated from the equations given with the diagram.

34

wheel of fortune



This circuit represents a simple 'wheel of fortune' or ten-sided die suitable for many games applications.

The wheel is 'spun' by pressing button S1, which causes pin 1 of the 7413 to go high. This starts the oscillator with the 7413-gate, and square wave pulses are fed to pin 14 of the four-bit counter IC2. The oscillator stops when S1 is released.

The counter IC2 counts the total number of pulses that the astable multivibrator has produced during the period that S1 was open. A sufficiently high frequency is chosen for the oscillator to ensure that the player cannot cheat by releasing S1 at a chosen moment.

The four-bit information from the IC2 is

fed to a BCD to decimal converter IC3. As long as the state of the counter DCBA is lower than or equal to 1001, one of the 10 outputs of IC3 is low, i.e. one of the LEDs lights up. If, for example the state of the counter is DCBA = 0110, then output 6 of IC3 will be low and D7 will light up. However the 7445 decodes only 10 of the 16 possible counter states; from 1010 ... 1111 all 10 outputs of IC3 are high and none of the LEDs are lit. This state may be used to indicate the end of a player's turn. IC3 may be replaced by a BCD-to-one-of-sixteen decoder, e.g. the 24-pin type 74154, along with half a dozen LEDs with series resistors. This will produce an electronic die with sixteen possible results.

35

stereo pan pot

This circuit offers the possibility of stereo image width control from stereo, through mono, to reverse stereo. The circuit comprises two emitter followers and a linear stereo potentiometer.

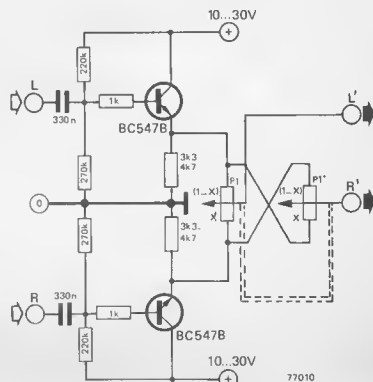
If x is the ratio of the resistance between the sliders of the pots and the lower ends of the pots to the total resistance then it follows that the outputs L' and R' are given by:

$$L' = R(1-x) + Lx$$

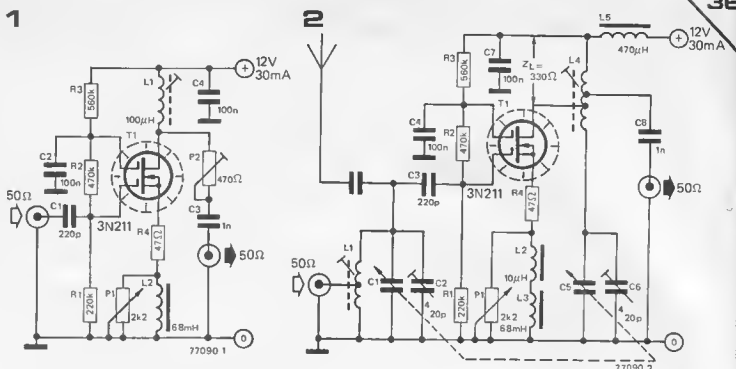
$$R' = Rx + L(1-x)$$

Therefore, when $x = 1$, $L' = L$ and $R' = R$ (normal stereo); when $x = \frac{1}{2}$, $L' = R' = \frac{1}{2}(L + R)$ (mono); when $x = 0$, $L' = R$ and $R' = L$ (reverse stereo).

The low output impedance of the emitter followers ensures that, when the potentiometer is in either the extreme clockwise or anticlockwise position, crosstalk travelling along the potentiometer tracks cannot appear at the outputs. Good channel separation in the stereo and reverse stereo modes is thus maintained.



R.F. amplifier with 100 dB dynamic range



This amplifier was designed to improve an existing receiver by replacing the original r.f. stage. The circuit utilises a dual gate MOSFET, has a dynamic range of 100 dB, and exhibits low intermodulation distortion over the range 100 kHz to 30 MHz. Incorporation of the amplifier into an existing receiver obviously varies, depending on the receiver, and cannot be discussed in detail but must be left to the individual constructor.

Figure 1 shows the test circuit which was used to measure the performance of the amplifier using a spectrum analyser. Two signals of equal amplitude at 5.2 MHz and 5.24 MHz were fed into the amplifier and the IM products were examined. With an input amplitude of 1.25 V p-p per input signal, photo 1 clearly shows that the IM products are at least -40 dB with respect to both output signals. The voltage gain of the amplifier is approximately four, with P1 set to minimum.

It was decided to incorporate a manual r.f. gain control into the amplifier, since this facility was present in the receiver which was to be modified. Varying the gain by changing the working point of the FET (as is common practice) was quickly rejected,

since it led to a large increase in intermodulation distortion. This is apparent from photo 2, which was taken with R3 removed from the circuit.

The final solution was to apply a variable amount of negative feedback to the FET source via P1. At DC, P1 is short-circuited by the low resistance of L2, so varying P1 can have no effect on the DC bias conditions. At radio frequencies, however, L2 presents a very high impedance, and the gain can thus be varied by adjusting P2. Photo 3 shows the low (-50 dB!) intermodulation products even with P1 at maximum resistance (minimum gain). P1 can vary the gain by a factor of 30 dB, and with P1 set to minimum gain input signals of up to 6 V p-p may be handled with the same low level of distortion.

Figure 2 shows a typical application of the amplifier in a receiver. L1/C1, C2 and L4/C5, C6 are the existing first and second tuned r.f. circuits of the receiver, the active part of the circuit (r.f. amplifier) being replaced by the MOSFET stage.

In view of the relatively large dissipation in the MOSFET (typically 300 mW) it should be fitted with a heatsink.

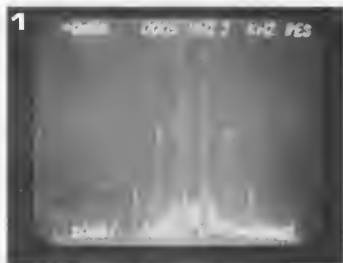


Photo 1. The output spectrum of the amplifier with two input signals of 1.25 V_{pp}. (P1 set for maximum gain).

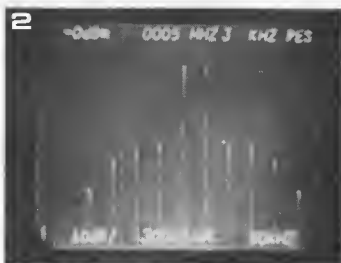


Photo 2. The output spectrum of the amplifier with the same signals as in photo 1, but with R3 removed. Although there is a reduction in gain, there is a considerable increase in the intermodulation products.

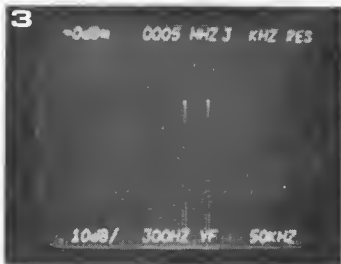
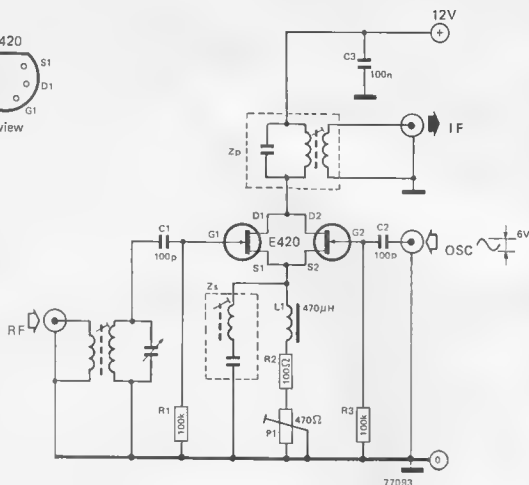


Photo 3. The same input signals as in photo 1, but with P1 set for minimum gain. The intermodulation distortion is 10 dB better.

high-level mixer



The dynamic range of a receiver is largely dependent upon the characteristics of the mixer. It is therefore crucial that large signals are processed by the mixer with a minimum of distortion, and that at the same time its noise figure should be as low as possible. When the noise figure is less than 10 dB for the frequency range from 0.1 to 30 MHz, and there is a conversion gain of 6 dB, then the mixer can be used directly as the input stage of the receiver.

For superhets with a fairly high intermediate frequency (e.g. 9 or 10.7 MHz) it simplifies matters if the RF- and oscillator-inputs of the mixer have a high impedance. The circuit described here fulfils these requirements: Two input signals, each 2.5 Vpp, produce an output signal with a third order IMD of -45 dB. With the optimum setting for P1, Z_S and Z_p the conversion gain is approx. 6 dB and the noise figure approx. 4 dB.

Although the circuit looks symmetrical, this is not quite the case. The input signal at G1 is present in attenuated form at both sources and this produces two drain signals in antiphase. However, these signals are not quite equal. This is equally true for the oscillator signal. This slight degree of asymmetry means that the input and oscillator signals will not completely cancel.

The ratio $Z_p:Z_S$ needs to be between 6 and 10 at the intermediate frequency. The simplest solution is to make Z_S smaller than

is thought necessary and to place it in series with a resistor.

Although this 'long-tailed pair' mixer can be found in most radio design handbooks, what is not often mentioned is that the circuit will fail to function satisfactorily without Z_S . This impedance is minimal at the intermediate frequency, and this results in narrow-band response of the mixer. This is more of an advantage than a disadvantage, since most IF-filters have a higher impedance outside the pass-band than in the pass-band, a fact which can often cause overloading at the mixer output.

The tuning procedure is as follows:

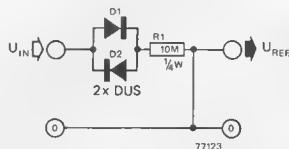
Z_S is omitted and an RF signal which is large enough for cross-modulation to be just audible, is fed in. P1 is then adjusted to minimum cross-modulation (if necessary the RF-signal should be increased further). Z_S is then added. If the component values are correct, then this should increase the value of the IF-signal without affecting the cross-modulation. Care should be taken to ensure that no IM occurs after the mixer stage!

If high-frequency measuring equipment is available, the procedure can be simplified. An HF signal generator, for instance, can be used to produce any desired amount of IMD; a spectrum analyser is an invaluable aid for those perfectionists who want absolute 'spot-on' alignment.

0 V voltage reference

This circuit will provide an accurate 0 V reference output. The input voltage can vary between -1000 V and +1000 V without detriment to the precision of the reference output.

This particular design approach is a major improvement over more conventional circuits, in that it results in an exceptionally low output impedance while at the same time being completely short-circuit proof.



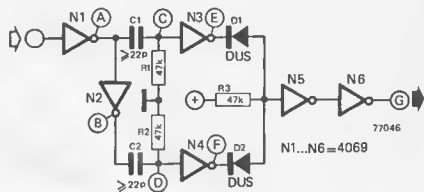
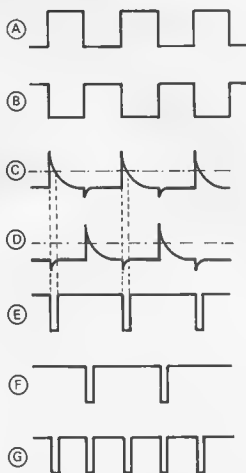
MISSING LINK:

Last-minute lab tests have shown that the performance can be improved still further by omitting D1, D2 and R1.

41

frequency doubler using 4069

A.M. Bosschaert



Using a single 4069 hex inverter IC, a frequency doubler can be constructed to give an output pulse train whose frequency is twice that of a squarewave input signal. The signal is applied to the input of N1. It should be a squarewave with a duty-cycle of approximately 50% at a level compatible with CMOS logic (3 – 15 V peak-to-peak depending on supply voltage). The input signal is buffered and inverted by N1, and inverted again by N2, so the outputs (A and B) of N1 and N2 are squarewave signals 180° out-of-phase. The output of N1 is differentiated by C1 and R1 and the output of N2 is differentiated by C2 and R2, giving two spike waveforms (C and D) 180° out-of-phase. These signals are buffered, inverted

and 'squared up' by N3 and N4 to give waveforms E and F. These are then combined in a NOR gate consisting of D1, D2, R3 and N5, and finally inverted by N6 to give the output waveform G, which has a frequency twice that of the input signal.

The circuit will operate over a wide frequency range. The upper frequency restriction is imposed by the fact that the width of the negative-going pulses E and F must be greater than the minimum pulse width that N3 and N4 will reliably transmit. Assuming that waveforms E and F have the minimum possible pulse width, as the frequency of the input signal increases the duty-cycle of the output signal will approach 50% as the pulses come closer together. When this situation is reached then the width of the positive output pulses is also the minimum that the 4069 will handle.

With the component values shown the width of pulses E and F is about 500 ns, so the duty-cycle of the output will be 50% when the frequency is 1 MHz, i.e. when the input frequency is 500 kHz.

42

digital capacitance meter with 555 timer

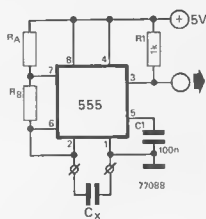
J. Borgman

Anyone possessing a frequency counter with a facility for period measurement can build this simple add-on unit to measure capacitance direct.

In the circuit shown the 555 is connected as an astable multivibrator, the period of which is given by $T = 0.7(R_A + 2R_B)C_X$. If the unknown capacitor is connected in the C_X position then, since R_A and R_B are fixed, the period is proportional to C_X , the unknown capacitor. The period of the multivibrator can be measured by the period meter and, if R_A and R_B are suitably chosen, this reading can be made to equal the capacitance in picofarads, nanofarads or microfarads. As an example, suppose the period meter has a maximum reading of one second and this is to be the reading for a capacitance of 1 μF . Then the total value of $R_A + 2R_B$ should be 1.43 M Ω .

A slight problem exists when measuring electrolytic capacitors around the 1 μF value. As shown above, for a reading of one second the resistance required is fairly high and errors may occur due to the capacitor leakage resistance. In this case it is probably better to opt for a reading of 1 second = 1000 μF , since the resistance values can be 1000 times smaller. If a seven decade counter is used that gives a reading of 1.000000 for one second = 1000 μF , then 1 μF will give a reading of 0.001000, which is still better than the accuracy of the circuit.

Some suitable values for R_A and R_B are given in the table. 1% metal oxide resistors should be used for these to give a reasonable



accuracy. Other values can be calculated to suit personal taste and the counter used.

When using the circuit the wiring capacitance of any jigs and fixtures used to hold the capacitor should be taken into account and subtracted from the reading. For this reason, such jigs should be of rigid mechanical construction so that the capacitance does not vary. For example, in the prototype it was found that the circuit was reading consistently 36 pF high due to wiring capacitance. This was therefore noted on the test jig so that it could be subtracted from all readings. Of course, when testing large value capacitors this small error is not significant.

R_A	R_B	C_X	T
1 k	220 Ω	1000 μF	1 s
1 M	220 k	1 μF (non-electrolytic)	1 s

43

add-on timer for snooze- alarm-radio- clock

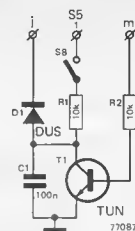
P.C.M. Verhoosel

This circuit will enable the digital clock published in Elektor No. 20 to be used as an interval timer that will switch on an appliance at a particular time and switch it off after a preset interval.

The circuit requires only three connections to the existing clock circuit, to points j, m and position 1 of S5, as shown. In addition, S6 must be replaced by a single-pole change-over switch with centre off position, for reasons which will become apparent.

The circuit functions as follows: when the clock is to be used as an interval timer S6 is set in the centre off position (this prevents the alarm output from activating the buzzer or the relay) and S7 is open. To set the interval timer, the start time is set (with S8 open) by turning S5 to position 3 and using S1 and S2 to set the desired alarm (start) time. S5 is then returned to position 1, S8 is closed and S1 and S2 are used to set the 'radio delay' time (max. 59 minutes), which is used as the interval time.

Until the desired start time is reached, 'alarm output' m will be low, T1 will be turned off and input j will be held high via D1 and R1, so the clock will display the selected interval time. When the start time is reached the alarm output will go high, turning on T1. The radio relay output will go high, energising the relay, and the 'radio delay' timer will start to run. At the end of the selected interval the 'radio delay' output will go low and the relay will drop out.



During the timing interval the clock will revert to normal time display, but the state of the interval timer can be examined by briefly setting S5 to position 4. The one disadvantage of this system is that it is not possible to read the actual time from the clock during the time the relay is not actuated, as opening S8 to revert to normal time display will also cause the relay to pull in. However, assuming that the interval timer is to be used while one is out of the house, this is not a great disadvantage.

To avoid cutting an extra hole in the clock case for S8 an alternative would be to replace S5 with a six-way switch. The sixth position of this switch would be connected to the top end of R1 in place of S8 and could then be labelled 'interval timer'.

44

TV games

Wherever there is a mass market for a complex digital circuit, an LSI chip is sure to appear. It should not come as a surprise that 'TV games' are no exception.

The chip used here, the AY-3-8500, offers six different games and includes scoring and sound effects. To simplify matters, all output signals are derived from a single clock frequency. Divider stages in the IC are used to 'produce' players, ball, boundary lines etc. The positions of the players are determined by the period times of two on-board monostable multivibrators.

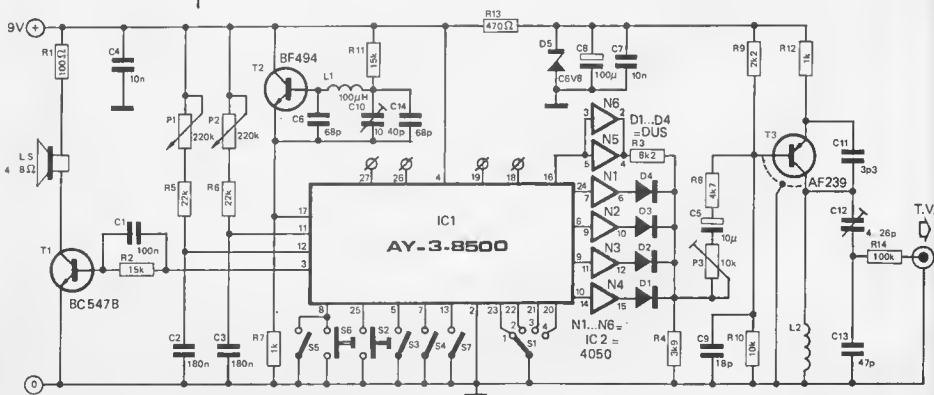
The circuit shown here will give four different games: Pelota, Squash, Hockey and Tennis. The chip itself is capable of two further games, but since they require a special (optical) gun it was decided not to include them in this simple circuit. The corresponding 'game select' pins (18 and 19) and the connections to the small additional

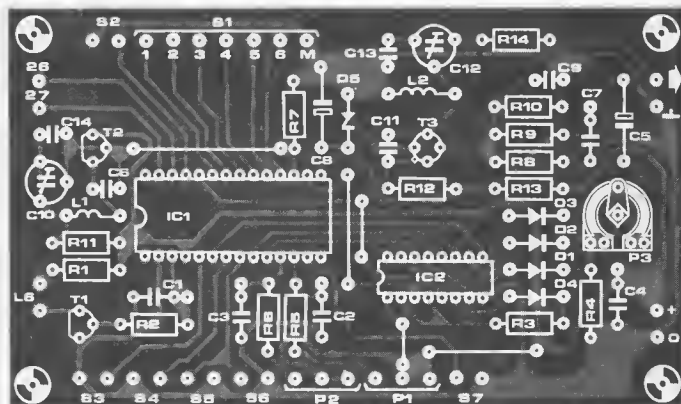
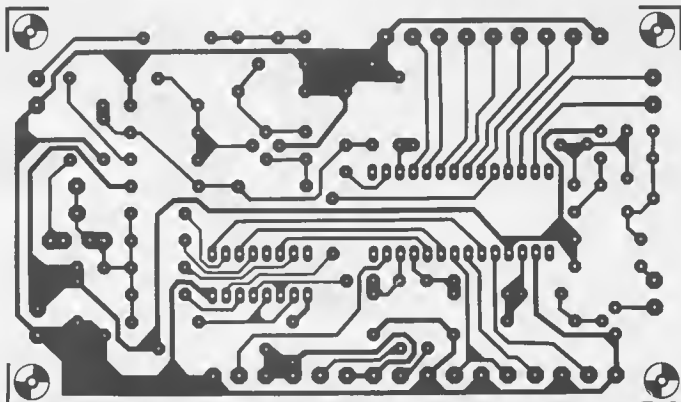
circuit required (pins 26 and 27) are brought out, however.

The complete unit, including an audio amplifier (T1), the clock oscillator (T2) and a VHF/UHF oscillator (T3) can be mounted on a small printed circuit board (EPS 77084). The power supply should be capable of delivering 9 V/100 mA.

P1 and P2 are the 'player position' controls. Initially, C12 can be set in the mid-position and the television set can be tuned through the low UHF band until the signal is located. If necessary, the signal can be moved up or down the band by readjusting C12. The next step is to adjust C10 until a stable picture is obtained; finally, the contrast can be adjusted according to personal taste with P3. Note that it is not advisable to set too bright a picture, as this may eventually cause damage to the picture tube.

The desired game is selected with S1; S2 is





used to reset the counters before the start of each game. S3, S4 and S7 are used to vary the degree of skill required to play the game: they offer a choice between two 'bounce-

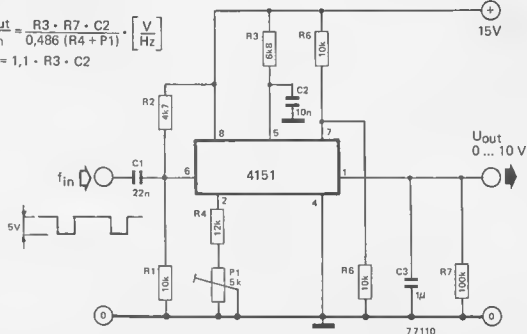
angles', two ball-speeds and two sizes of player. S6 is used to 'serve'; alternatively, S5 can be closed whereupon the ball will be served automatically.

45

frequency-voltage converter

$$\frac{U_{out}}{f_{in}} = \frac{R3 \cdot R7 \cdot C2}{0,486 (R4 + P1)} \cdot \left[\frac{V}{Hz} \right]$$

$$T1 = 1,1 \cdot R3 \cdot C2$$



This frequency-voltage converter is distinguished by its markedly linear conversion ratio. With the given component values the conversion ratio of the circuit is 1 V/kHz. If a DC voltage is applied to the input (0 Hz) then the output voltage is 0 V. The duty cycle of the squarewave input signal has no effect upon the conversion ratio. However, if sinusoidal signals are to be converted to a DC-voltage, then the converter-IC should

be preceded by a Schmitt trigger. Other conversion ratios can be calculated using the formulae shown in the diagram. The circuit can also be connected to the output of a voltage-frequency converter and used as a means of transmitting DC signals over a long cable without the cable resistance attenuating the signal.

RAYTHEON product specifications

46

common-base virtual earth mixer

The most usual form of virtual-earth mixer consists of an inverting amplifier with the inputs to be mixed (or more accurately summed) being fed via resistors to the virtual earth point at the inverting input. However this unusual circuit utilises a single transistor operated in common-base configuration, and does not invert the input signals.

T1 receives a constant base bias voltage from R1, D1 and D2, and thus the emitter voltage is also held constant at about 0.6 V. A

constant current of $\frac{0.6}{R_2}$ thus flows through

R2. Assuming, for simplicity, that the mixer is dealing with AC input signals, under quiescent (no signal) conditions the DC current through R2 is almost entirely supplied by T1 and is almost equal to the collector current.

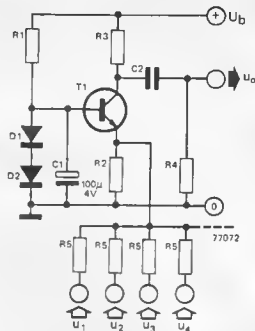
If an AC signal is applied to one of the input resistors R5 then an AC current $\frac{U_n}{R_5}$ will flow

through R2. Since the total current through R2 remains constant the proportion of that current supplied by T1 will vary in sympathy with the input signal and an AC output signal will appear at the collector of

T1. The gain of the mixer is $\frac{R_3}{R_5}$ so, assuming all the R5's are the same, the output

voltage $U_0 = \frac{R_3}{R_5} (U_1 + U_2 + U_3 + \dots + U_n)$.

As the emitter of T1 remains at constant voltage it is an almost perfect virtual earth summing point. The distortion factor of the mixer is determined almost exclusively by the linearity of the current gain in the common-base configuration, which is $\frac{h_{fe}}{1 + h_{fe}}$.



If a high-gain transistor (large h_{fe}) is used then the current gain will be almost unity and variations in h_{fe} will have little effect, so the distortion will be low.

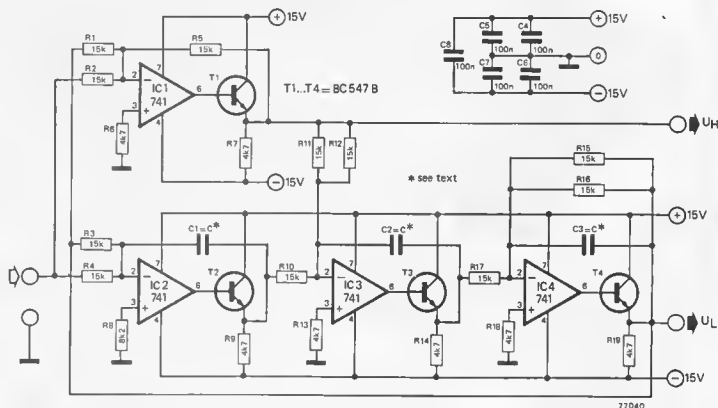
The input resistance of the circuit is equal to R5, so R5 must obviously be made equal to the desired input resistance. R3 is chosen equal to $\frac{R_5}{n}$, where n is the number of inputs.

Finally, for optimum results R2 should be made equal to $\frac{1.2 \times R_3}{U_b}$. This fixes the DC collector current of T1 and sets the collector voltage to around half supply.

As an example, if R5 is 33 k and there are four inputs the value of R3 is 8k2. With a supply voltage of 15 V R2 is thus 680 Ω (these are nearest preferred resistors to actual values).

47

symmetrical constant- voltage cross-over filter



This circuit is intended as a practical supplement to earlier articles on the subject of constant voltage filters (see Elektor 25/26 'active loudspeaker-crossover filters'; and Elektor, Elektor 26). The design is based on a circuit published in the article 'Active and passive filters as loudspeaker crossover networks' JAES, June 1971. In the same article there are a number of other circuits for constant-voltage filters with differing symmetrical and asymmetrical filter slopes.

The circuit consists of three integrators and a summing amplifier, which together form a constant-voltage filter with an ultimate slope of 12 dB per octave. The sum of the voltages U_H (for the high-pass filter) and U_L (for the low-pass filter) is amplitude and phase

constant, and therefore does not vary with frequency. The crossover frequency f_0 is given by: $f_0 = 1:2\pi RC$, which implies that $C = C_1 = C_2 = C_3 = 1:2\pi f_0 R$, where R is 15 k. For a crossover frequency of 500 Hz, for example, C will equal 21.2 n. An ordinary 741, provided with an emitter follower at the output, will suffice as a choice of op-amp. Symmetrical supply voltages of ± 15 V are necessary; current consumption is less than 25 mA.

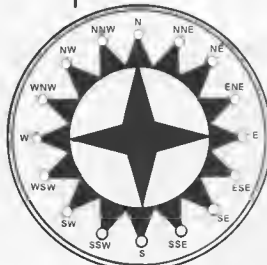
The amplitude response curves for U_L and U_H differ from the normal Butterworth curve in as much as, for U_L , a peak of approx. 4 dB appears at a frequency of $0.8 f_0$, whilst an identical peak appears at $1.2 f_0$ in the curve for U_H .

48

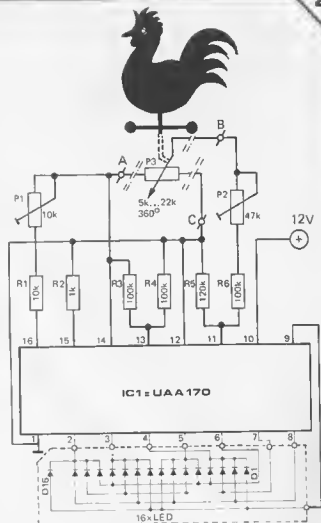
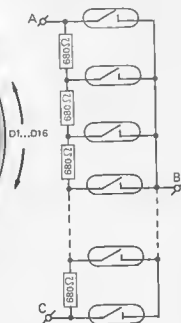
electronic weathercock

Until recently, finding out which way the wind is blowing has always necessitated putting on one's shoes and stepping outside the door, thereby exposing oneself to the vagaries of the British climate. However with a little technical ingenuity, it is possible nowadays to know the precise direction of the wind without leaving the comfort of one's fireside. The electronic weathercock functions by connecting the vane to a potentiometer which turns with the vane. The voltage at the slider of the potentiometer is then proportional to the angle through which the vane is turned by the wind. The size of this voltage (and hence the direction of the wind) may be displayed in digital form using a UAA 170 and 16 LEDs.

The circuit is designed so that there is a smooth interchange between the LEDs. Potentiometer P1 controls the brightness of the LEDs, whilst P2 is set such that, when the voltage at the slider of P3 (which is connected to the vane) is at a maximum, then D16 lights up. Further details regarding the UAA 170 may be found in *Elektron* 12, April 1976.



77013



one solution is to use sixteen reed relays, each of which is enabled whenever a magnet connected to the vane passes over the relay. In this case a resistance divider replaces the potentiometer. Readers who are adept at making very small printed circuit boards, may like to replace the carbon track of a conventional potentiometer by a small 16-segment circuit board and connect each segment to the resistance divider. The supply does not need to be stabilised, since the IC has an internal reference voltage output (pin 14) which is (gratefully) utilised. The maximum current through an LED is approx. 50 mA, thus a suitable supply would be a transformer producing 100 mA with a voltage of 9 or 12 V. The circuit is completed by a bridge rectifier and a 470 μ 25 V electrolytic capacitor.

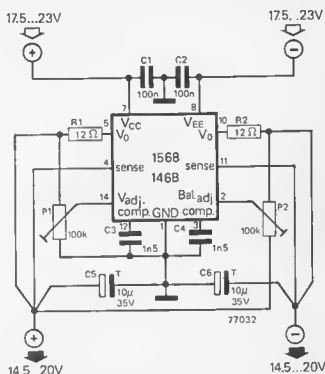
49

 ± 15 volt regulator

Using IC 1568 or 1468 (from, among others, EXAR) and only a small number of external components, it is possible to produce a symmetrical, current-regulated supply voltage of plus and minus 15 volts.

The circuit is intended as an 'on card' supply, and is not particularly suited for experimentation, since the maximum dissipation of the IC is not particularly high (max. 1 W). With the circuit arrangement as shown in the figure, it is not advisable, in view of this dissipation value, to select input voltages much greater than those indicated (i.e. 3 V above the output voltage). It goes without saying that the IC will not be able to tolerate shorting the outputs for long. The current is limited as soon as the voltage drop across either of the two resistors R1 and R2 exceeds 0.6 V. By means of P1 the output voltage may be varied between 14.5 and 20 V (always assuming that the input voltage is sufficiently high). The positive and negative voltage can be matched exactly using P2. Capacitors C1...C4 are needed to guarantee the stability of the supply, and should be positioned as near as possible to the IC. Some further details: the 1568 differs from the 1468 in having a slightly narrower tolerance with respect to the value (0.2 compared to 0.5 V) and match of the output voltages (150 compared to 300 mV).

The maximum input voltage is 30 V, and the

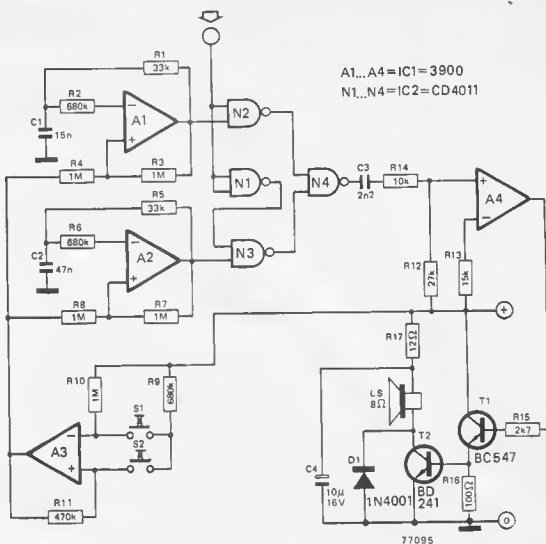


max. current 100 mA. A change in the load of 50 mA causes a variation of approx. 3 mV in the output voltage. For a current of 50 mA the minimum voltage drop across the regulator is at least 2.5 V. The noise suppression is then around 75 dB, and the stability of the output voltage is better than 1% for a variation in temperature of 75°C. The noise at both outputs is less than 0.1 mV.

52

audible logic probe

H. Käser



This logic probe provides an audible rather than a visual indication of logic state by producing a high-frequency audio tone for a logic '1' state and a low-frequency tone for a logic '0' state.

The logic input signal is fed to N1 and N2. If the input is high then N2 will pass the high frequency signal from the oscillator built around A1. If the input is low then N2 will block, but the output of N1 will be high so N3 will pass the low frequency signal from the oscillator built around A2.

Depending on the input state one or other of these signals is fed through N4 to the input of a differentiator built around A4. This produces a train of short pulses from the squarewave input signal and these are fed to an audio amplifier comprising T1 and T2.

The use of short pulses ensures a high peak audio output while keeping the average current consumption low.

To avoid the annoying 'bleeping' of the circuit when measurements are not being taken both oscillators may be switched on and off by a flip-flop constructed around A3, which is controlled by two push buttons S1 and S2.

If the circuit is to be used exclusively with TTL circuits then N1 to N4 should be a 7400 IC and the supply voltage should be +5 V, which can be derived from the circuit under test. If it is to be used with CMOS ICs then N1 to N4 should be a 4011 IC, and the circuit will operate over supply voltages of 5 to 10 V at a current consumption of between 4 and 10 mA.

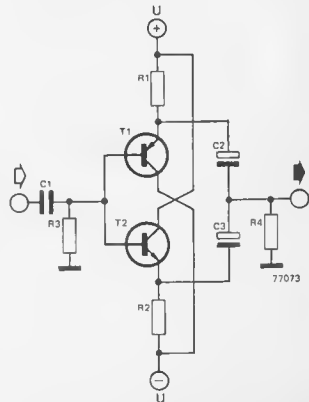
53

complementary emitter follower

This circuit presents an interesting alternative method of constructing a low-distortion buffer or output stage for use at low output powers. The quiescent current flowing through T1 and T2 is determined solely by the value of U and of R1 and R2 respectively. This contrasts with conventional circuits where the bases of T1 and T2 are connected to one another by means of a diode network. The current supply of the diodes normally has an unfavourable influence on the input impedance (unless bootstrapping is used) causing variations in the quiescent current.

In this circuit the quiescent current through T1 equals $\frac{U-0.6}{R_1}$, and that through T2 is $\frac{U-0.6}{R_2}$, assuming that the current gain of T1 and T2 are so high (or closely matched) that the voltage drop across R3 is negligible. Normally R1 is given the same value as R2. The relative values of C2, C3 and R4 determine the lowest frequency at which the circuit will function.

If T1 and T2 have the same current gain and R1 equals R2, then no DC voltage is produced across R3, and C1 may be omitted. If the circuit is fed from an op-amp then both C1 and R3 may be omitted.

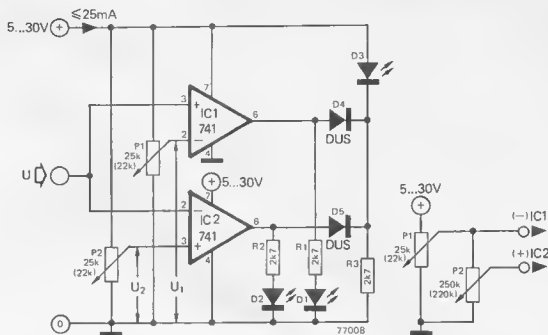


The circuit is intended as a class-A buffer or output stage. The maximum class-A output power dissipated in R4 is $I^2 R_4$, where I is $\frac{U-0.6}{R}$ assuming that R4 is smaller than $R = R1 = R2$.

56

tri-state
voltage
comparator

R.Sloan



This circuit will compare an unknown input voltage with two preset reference voltages and display the result on one of three LEDs. IC1 and IC2 function as comparators. If U is less than U_2 then the output of IC2 will be high and D2 will be lit. If U is greater than U_2 but less than U_1 then the outputs of IC1 and IC2 will both be low and D3 will be lit. If U is greater than U_1 then the output of IC1 will be high, IC2 will be low and D1 will be lit.

Of course, the foregoing assumes that U_1 is greater than U_2 . This can be achieved by correct adjustment of P1 and P2. Alternatively, to ensure that U_1 is always greater than U_2 P1 and P2 can be arranged as shown

with P2 deriving its supply from the slider of P1. Note that P2 is now 250 k. With this arrangement there will be some interaction between the two potentiometers.

The circuit makes an ideal battery state indicator for a car. P1 and P2 can be adjusted so that D2 lights if the battery voltage falls below say 11 V, D3 lights between 11 and 13 V and D1 lights above this.

Many types of op-amp IC will work in this circuit, but if a quad Norton op-amp such as LM3900 is used then a 100 k resistor should be placed in series with the + and - inputs of each op-amp.

57

level shifter

It is often necessary, particularly when experimenting with circuits, to make connection between the output of one circuit and the input of another which is at a different DC level. If the signals involved in the circuit are AC signals this is no problem, a capacitor can be used to isolate the DC levels while allowing AC signals to pass. However, when dealing with DC or very low frequency AC signals the solution is not so easy, and it is in these cases that this little gimmick will prove useful.

The circuit consists simply of an op-amp connected as a voltage follower whose quiescent output voltage can be set to any desired level within the output range of the op-amp.

Input A is connected to the output of the circuit in question while the output is connected to the input of the circuit which it is feeding. Input C is grounded, while input B is connected to a DC voltage equal to the difference between the input voltage of the second circuit and the output voltage of the first.

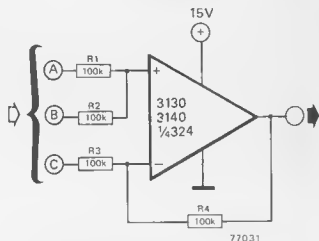
It can easily be proved that this works! Firstly, voltages appearing at the non-inverting input of the op-amp are amplified

$$\text{by a factor } \frac{R_3 + R_4}{R_3} = 2.$$

Secondly, suppose the output voltage of the first circuit is V_A and the input voltage of the second circuit is V_1 . The voltage V_B applied to input B is thus $V_1 - V_A$. The voltage appearing at the junction of R1 and

$$R_2 \text{ is thus } V_A + \frac{V_B - V_A}{2}.$$

The voltage appearing at the op-amp output is twice this, i.e. $V_A + V_B$. But since $V_B = V_1 - V_A$ this equals V_1 , the input voltage of the second circuit. Obviously, if V_1 is less than V_A then V_B



will be a negative voltage.

Despite the difference in input and output levels the circuit functions as a voltage follower in that any change in the voltage at input A will produce the same voltage change at the output.

The circuit can also be used as an inverter. In this case the signal is fed to input C, B is grounded and A is fed with a DC reference voltage. To see what voltage must be applied to A it is simplest to treat the circuit as a unity gain differential amplifier. The output voltage V_O is equal to the difference between the voltages at the non-inverting and inverting inputs i.e. $V_O = V_A - V_C$ so $V_A = V_O + V_C$, i.e. input A must be fed with a voltage that is the sum of the voltage at C and the required output voltage. Any change in the input voltage at C will produce the same change at the output, but of opposite polarity.

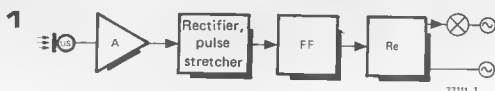
Two points must be noted when using this circuit. Firstly, care must be taken not to exceed the common-mode input rating of the op-amp used, especially with a single-ended (asymmetric) supply. Secondly, the values of R1 to R4 should be at least ten times the output resistance of the circuit feeding the level shifter to avoid excessive loading of the output.

ultrasonic receiver

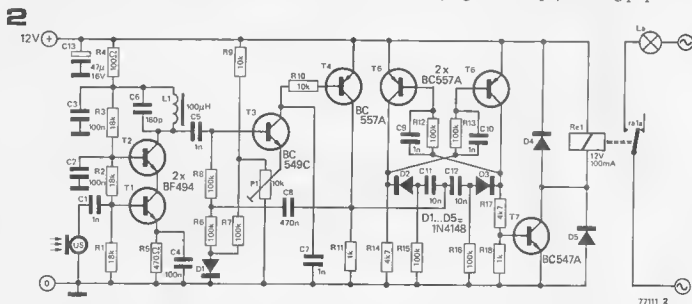
This receiver is intended to be used with the US transmitter described elsewhere in this issue. The input signal is fed to a cascade amplifier comprising T1 and T2, which amplifies it approximately 2000 times. T3 functions as a rectifier, and T4 amplifies the rectified signal, which is used to trigger a flip-flop comprising T5 and T6. This will be set on one US burst and reset on the next, thus turning T7 on and off to successively energise and de-energise the relay.

To reduce the circuit's sensitivity to multiple triggering (caused principally by Doppler-shift) positive feedback is provided via C8 causing T3 and T4 to operate as a monostable. This ensures that only one output pulse is generated for each received pulse and

prevents spurious triggering of the flip-flop. To set up the receiver the following procedure should be observed. Turn the slider of P1 towards the 0 V rail. This should cause the relay to pull in and drop out at random. P1 is then adjusted until this just ceases, when the receiver sensitivity will be at a maximum. Activating the transmitter should now energise the relay. The system will operate at distances of up to eight metres. If this range is too great then it may be reduced by suitable adjustment of P1. The receiver should be set to the minimum range required for a particular application, as too great a sensitivity may cause spurious triggering by normal sounds which have an ultrasonic content, e.g. handclaps, rustling paper etc.



77111 1



77111 2

ultrasonic
transmitter
for remote
control

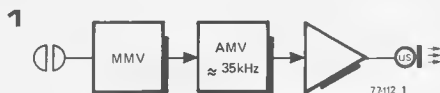
This simple ultrasonic (US) transmitter uses only one CMOS IC and a few discrete components, and will generate a short pulse of ultrasound. This can be used to trigger an ultrasonic receiver (such as the one described elsewhere in this issue) to activate a relay or other circuit.

When the touch contacts on the input of N1 are bridged by a finger the output of N1 will go low and the output of N2 will go high, holding the input of N3 high via C2 for about 60 milliseconds.

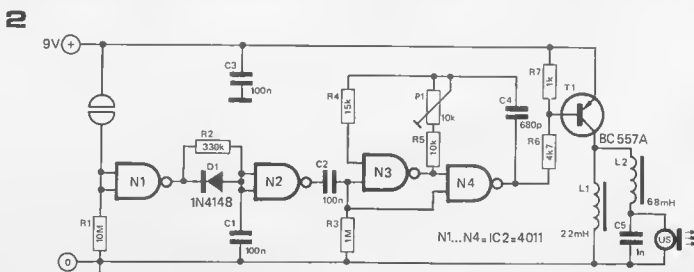
During this time the astable multivibrator comprising N3 and N4 will oscillate at about 40 kHz (adjustable by P1). Since the

output of N4 can supply little current, drive to the US transducer is provided by T1 which feeds the resonant circuit L2/C5. This is tuned to around 40 kHz, which is the resonant frequency of most US transducers. Although only a 9 V supply is used, the 'Q' of the resonant circuit ensures that a high drive voltage appears across the transducer (up to 100 V), and a range of up to eight metres can be achieved in conjunction with the aforementioned receiver.

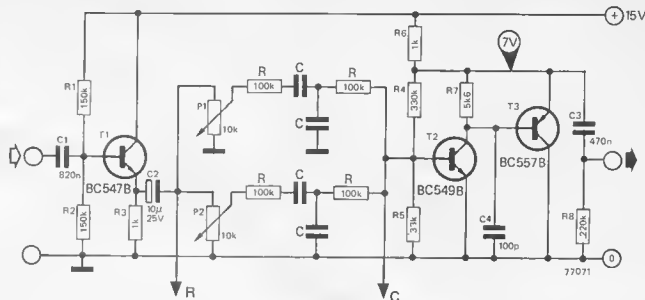
As the circuit consumes virtually no power except when actually transmitting, no on-off switch is required. Almost any 40 kHz US transducer can be used.



77:112 1



72112 2

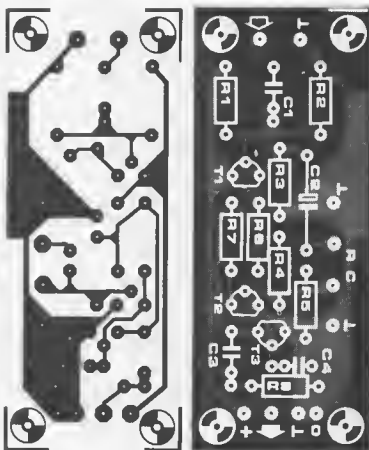


This simple equaliser is intended mainly for tailoring of room acoustics in such applications as disco and p.a. work, and for sound effects in electronic music. It is not intended for hi-fi use as more sophisticated circuits are needed to give satisfactory results in this application.

The circuit comprises an emitter follower T1 feeding a number of Wien networks, each of which passes a band of frequencies about its centre frequency. P1, P2 . . . etc. vary the proportion of the total signal that is fed to each Wien network and hence the proportion of each selected frequency band that appears at the output. By using a number of Wien networks with centre frequencies spaced at suitable intervals throughout the audio spectrum it is possible to boost or cut selected bands of frequencies, and thus adjust the response of the equaliser to compensate for room acoustics etc.

The output of each Wien network is fed to a summing amplifier consisting of T2 and T3, which has a gain of three to overcome the attenuation of three introduced by the Wien networks at their centre frequencies.

For most purposes five Wien networks should be sufficient with centre frequencies of 40 Hz ($C = 39$ n), 155 Hz (10 n), 625 Hz (2n2 in parallel with 330 p), 2.5 kHz (680 p), 10 kHz (160 p).



EPS 77071

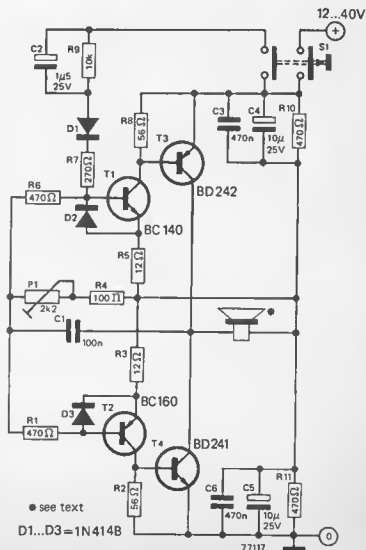
This 'inaudible' car horn is intended for warning four-footed pedestrians of imminent danger, without needlessly scaring the (hopefully) better-behaved two-footed variety.

Basically, the unit is a power multivibrator that oscillates at a frequency above the human hearing range – but clearly audible to the canine ear. The correct frequency can be set with P1. Bear in mind that young people can usually hear higher frequencies! R7, R9, C2 and D1 are required to start up the oscillator by passing a short current pulse into the base of T1. The only disadvantage of this type of circuit is that power must be applied 'instantaneously' – it will not work if the supply voltage rises slowly to its final value. However, if the unit is connected to a car battery, depressing S1 will reliably start the multib.

The minimum loudspeaker impedance is 4 Ω . On a 12 . . . 14 V supply the unit will deliver 5 W into this impedance. Alternatively, on a 40 V supply it will deliver 25 W into 8 Ω .

Not many tweeters can withstand this sort of drive level for long, so it is not advisable to use the horn for longer than a few seconds at a time.

As a final note: the unit can also be used to chase stray dogs out of the garden – and it is certainly more humane than throwing stones



• see text

D1...D3=1N4148

62

minireg
power supply

Although it utilises only two transistors and eight other components, this simple stabilizer will supply currents up to about 4 A and is equipped with foldback current limiting.

The circuit operates as follows: ignoring R1 for a moment, current from the output of the supply flows through D1, D2, R3 and P1 to ground. Due to the forward voltage drop of D1 and D2 the emitter of T2 is always biased about 1.2 V lower than the output voltage. Should the output voltage tend to rise the emitter voltage of T2 would rise by the same amount, but since the base is fed from the potential divider P2/R4 the base

voltage will rise by only $\frac{R_4}{P_2 + R_4}$ times this

amount. The base-emitter voltage of T2 will thus tend to fall and T2 will draw less current from R2. The base-emitter voltage of T1 will thus fall and T1 will tend to turn off, so the output voltage of the supply will fall. Should the output voltage tend to fall the reverse will occur. The base-emitter voltage of T2 will tend to increase. T2 will turn on harder, which in turn will turn T1 on harder, and the output voltage will be restored to its original value.

The output voltage of the power supply is given by

$$V_o = (V_z - 0.6) \cdot \left(\frac{R_4}{P_2} + 1 \right)$$

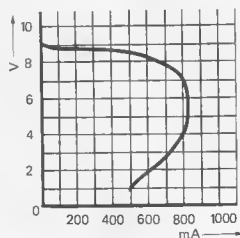
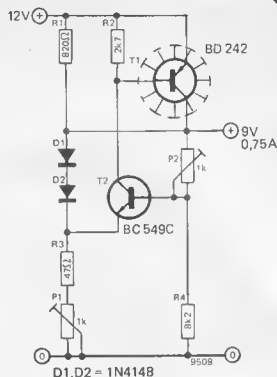
Where V_z is the forward voltage drop of D1 plus D2.

As the output current of the supply increases the current through T2 also increases as it turns on T1 harder and harder. The voltage drop across R3 and P1 will therefore increase, and the current through D1 and D2 will decrease. When the current has decreased so far that D1 and D2 are in the non-linear region of their forward transfer curve the voltage across D1 and D2 will begin to fall, and hence the output voltage will fall since the V_z term in the above equation is decreasing. The output current will fold back as shown in the graph.

The maximum output current is given approximately by

$$I_{max} = \frac{(V_o - V_z) hFE T_1}{R_3 + P_1} (A)$$

where $hFE T_1$ is the DC current gain of T1. With an average BD242 having a gain of about 25 the maximum output current can be adjusted from a few hundred mA to about 4 A with the component values shown.



However, using the equations given it is not difficult to redesign the power supply for other output voltages and currents.

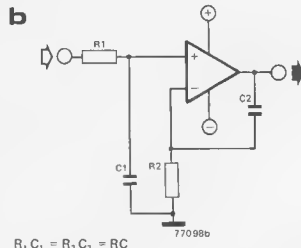
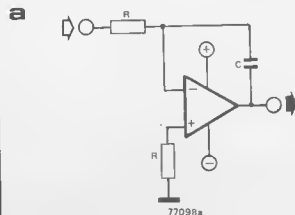
Resistor R1 is necessary to ensure that the circuit starts up reliably. If R1 were omitted then, on switch-on, T1 would be turned off and the circuit would fail to start. R1 provides base current to T2 which ensures that the circuit starts. The value of R1 should be the largest value at which the circuit still starts reliably.

If the circuit is to be used for lower currents than that specified then a lower power device may be used for T1. For currents up to about 50 mA a TUP may be used, provided the difference between the input and output voltages is not more than two or three volts. For currents from 50 to a few hundred milliamps a medium power device such as a BC143 could be used.

63

non-inverting
integrator

A drawback of conventional integrator circuits (figure a) is that the R-C junction is at virtual earth; this means that C appears as a capacitive load across the op-amp output, a fact that may adversely affect the stability and slow rate of the op-amp. Since the non-inverting character of an integrator is of minor importance in many applications the circuit shown in figure b offers a viable alternative to conventional arrangements.



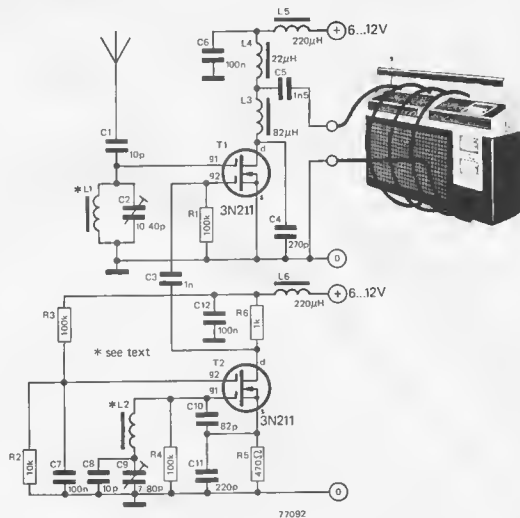
$$R_1 C_1 = R_2 C_2 = RC$$

This integrator, unlike that in figure a, is non-inverting. The time constants $R_1 C_1$ and $R_2 C_2$ should be equal.

If both R_1 and C_1 , and R_2 and C_2 are transposed then the result is a non-inverting differentiator.

For correct offset-compensation R_1 and R_2 should have the same value.

64

short-wave
converter

This frequency converter enables a normal medium wave radio to tune the short wave bands from 2 to 35 MHz. A MOSFET mixer and BFO are used to convert the frequency of the input signal to a frequency at the top end of the medium wave band (800 to 1600 kHz) which can be picked up by the ferrite aerial of the receiver.

A telescopic aerial of about one metre length should be used for the converter. A defunct car aerial with the cable removed is ideal, and can be picked up for next to nothing at any car scrapyard. The shortwave signal is fed from the aerial via C1 to the resonant circuit L1/C2 which tunes the aerial input, and thence to gate 1 of a dual gate MOSFET T1, which functions as a mixer.

T2 is the BFO and functions as a Clapp oscillator tuned by L2 and C8...C11. The BFO signal is fed to the second gate of T1. The mixer output is taken to a coil which consists of a few turns of insulated wire wrapped around the case of the MW receiver to feed the signal into the receiver's ferrite aerial. The MW receiver should not be placed too close to the converter as harmonics from

the receiver's local oscillator may be picked up by the converter.

To use the converter the MW receiver is tuned to about 1200 kHz and C9 is adjusted until short wave stations can be heard. C9 is used to tune the BFO so that 1200 kHz on the MW receiver corresponds to the centre of the desired short wave band i.e. by tuning the receiver from 800 kHz to 1600 kHz the entire band can be covered.

Once a station is tuned in C2 can be adjusted to give maximum signal strength.

Values of L1 and L2 for the various short wave bands are given in table 1.

Table 1

Frequency band (MHz)	L ₁ (μH)	L ₂ (μH)
2 ... 2.8	120	100
2.8 ... 4.0	56	56
4.0 ... 5.8	27	33
5.8 ... 8.3	15	18
8.3 ... 11.9	6.8	8.2
11.9 ... 17.0	3.3	4.7
17.0 ... 24.4	1.5	2.2
24.4 ... 35.0	0.82	1

65

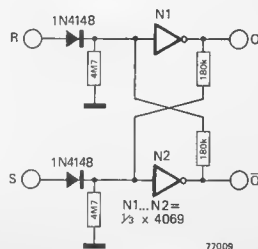
positive-
triggered
set-reset
flip-flop
using
inverters

The standard set-reset flip-flop circuit consists of two cross-coupled NAND gates and is set and reset by applying a logic '0' level to the appropriate input. The circuit shown in the figure is triggered by a logic '1' and uses inverters.

Assume that initially both inputs are low and the Q output is high. The input of N1 is also pulled high via the 180 k resistor, so the Q output is low, which holds the input of N2 low. If a logic '1' is applied to the S input the Q output will go low, pulling the input of N1 low, and the Q output will go high, thus holding the input of N2 high even if the S input subsequently goes low. Applying a logic '1' to the R input will reverse the procedure and reset the flip-flop.

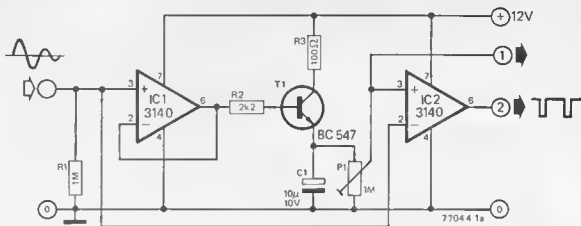
The circuits feeding the inputs of the flip-flop should be capable of providing a logic '1' level into a 180 k load, which normal CMOS circuits are capable of doing.

Reference: RCA Application Notes.



auto trigger
level control

1a



Oscilloscopes, frequency counters and other instruments triggered by AC signals almost invariably have a manual trigger level control, to adjust the point on the waveform at which triggering occurs. When making measurements where the signal level varies, for example at different places in a circuit, it is tedious to have to make frequent adjustments to this control.

The circuit described here provides a trigger signal at a fixed percentage of the peak input level, irrespective of what that level is, so the frustration of having the trace disappear from an oscilloscope when the signal level falls below the trigger level is avoided.

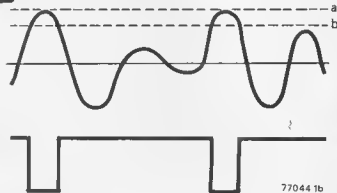
The circuit consists basically of a peak rectifier that provides one input of a comparator with a DC voltage equal to a fixed percentage of the peak signal level. The other input of the comparator is fed with the signal. When the signal level exceeds the DC reference level the comparator output will go low. When it falls below the reference level the comparator output will go high.

The peak rectifier consists of IC1 and T1. On positive half cycles of the signal waveform the output of IC1 will swing positive until T1 starts to conduct, after which IC1/T1 will act as a voltage follower, charging up C1 to the peak value of the signal.

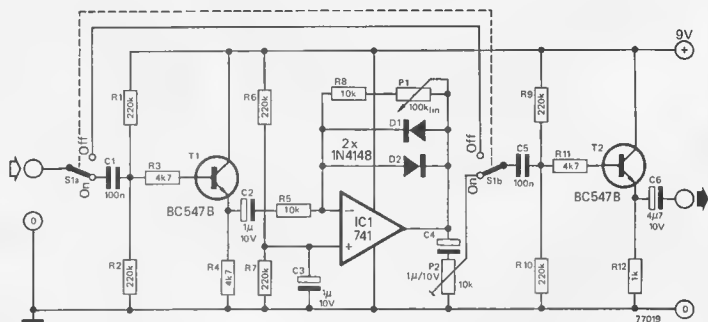
A portion of this voltage is taken from the slider of P1 and applied to the non-inverting input of IC2, which functions as a comparator. The AC signal is fed to the inverting input. When the signal level exceeds the reference voltage the comparator output will go low; when the signal level falls below the reference level the comparator output will go high. (see figure 1b)

P1 may be used to set the trigger level to any desired percentage of the signal level. The DC level at the slider of P1 may also be fed to the comparator input of an existing trigger level circuit. In this case this circuit should have a high input impedance to avoid discharging C1. Alternatively the output from P1 can be buffered by an op-amp connected as a voltage follower.

1b



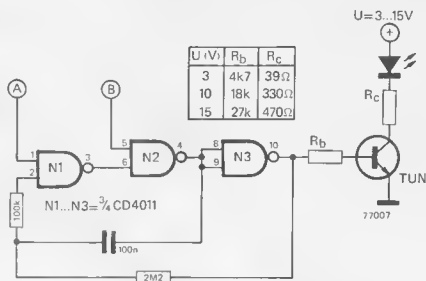
fuzzbox



The fuzzbox is an indispensable piece of equipment for the electric guitarist. This electronic device limits the guitar signal and produces a clipped waveform which, as is well known, contains a large number of harmonics. The guitar therefore produces a much richer sound. Many commercial fuzz amps suffer from the drawback that they may only be used with guitars which have pickups with low output impedance. This is not the case with the circuit described here. At the input is an emitter follower which acts as a buffer between the guitar output and the limiting amplifier and ensures a high input impedance. Operational amplifier IC1 is used to limit the input signal. The gain of

this amp and therefore the degree to which it limits the signal may be adjusted by potentiometer P1. When reverse parallel connected diodes D1 and D2 are conducting then the fuzz effect is produced. At the output there is another emitter follower which feeds the distorted guitar signal to the power amplifier at low impedance. Thus cable capacitance, even with a long cable, does not affect the high frequency response. By means of P2 the output signal of the limiting amp may be adjusted to suit any guitar amplifier. Switch S1, which is used to switch the fuzzbox on and off, can be conveniently mounted in a foot pedal.

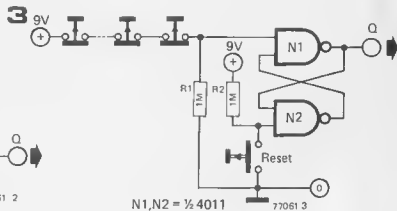
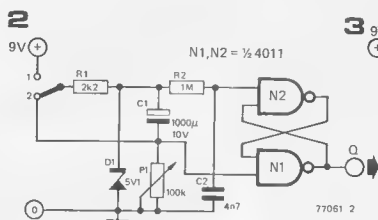
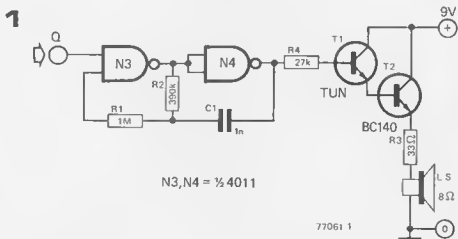
68

LED
logic flasher

The condition of the LED is determined by the logic states of the two inputs A and B. If A is low and B is high then the LED will be lit continuously. If B is low then the LED will be extinguished, irrespective of the state of A. If A and B are both high then the astable multivibrator comprising N1, N2 and

N3 will start to oscillate and the LED will flash at about 3.5 Hz. Component values are given for supply voltages of 3, 10 and 15 V. At the maximum supply voltage of 15 V the current consumption is less than 25 mA. Source: RCA CMOS Application and design ideas.

69

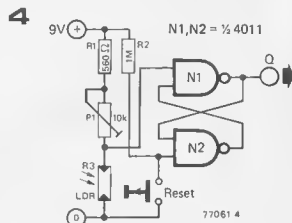
CMOS
alarm circuits

Because of their low cost, high input resistance, good noise immunity and wide supply voltage range CMOS logic circuits lend themselves to the construction of cheap and reliable alarm circuits for various applications.

Figure 1 shows a basic alarm oscillator constructed around two CMOS NAND gates. As long as input Q is low the circuit remains inactive. When input Q goes high the circuit begins to oscillate, switching T1 and T2 on and off and producing an alarm signal from the loudspeaker.

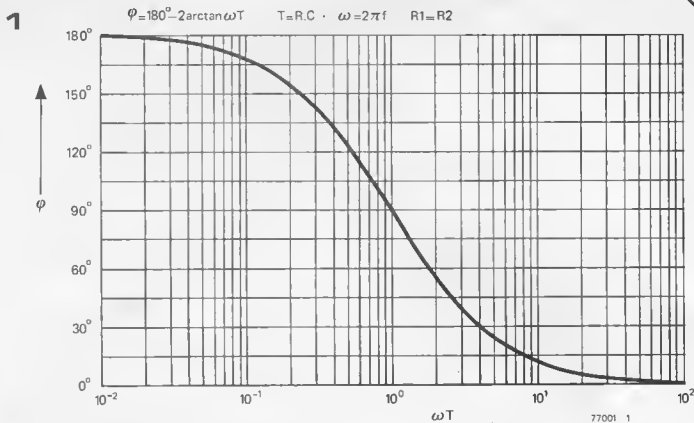
Figure 2 shows a circuit for triggering the alarm after a preset time delay that can be varied between one second and one minute. On switch-on the input of N2 is briefly held low by C2, so the flip-flop is reset and the Q output is low. C1 now charges via P1 so that the input voltage of N1 falls until the flip-flop is set and the Q output goes high.

Figure 3 is an alarm circuit that is triggered when a circuit is broken, this is particularly useful in burglar alarm systems where several switches can be connected in series. The input of N1 is normally pulled high via the switches, but if a switch is opened the input of N1 will be pulled down by the resistor,



setting the flip-flop and triggering the alarm. If the resistor is connected up to + supply and the switches are connected in parallel down to ground then the alarm can be triggered by closing a switch.

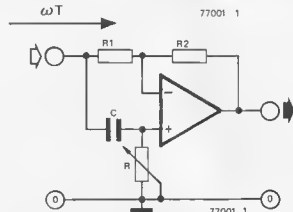
Figure 4 shows an alarm circuit that responds to light. In darkness the resistance of the LDR is high and the input of N1 is pulled high by R1 and P1. If light falls on the LDR the resistance falls and the input of N1 is pulled down, setting the flip-flop and triggering the alarm.



In contrast to lowpass or highpass filters, the gain of an all-pass filter remains constant over the range of frequencies at which it is used, but it does introduce a frequency-dependent phase shift. A number of all-pass filters may be cascaded to produce a phasing unit for use in electronic music. The phasing effect is produced by phase-shifting a signal and then summing the original and phase-shifted versions of the signal.

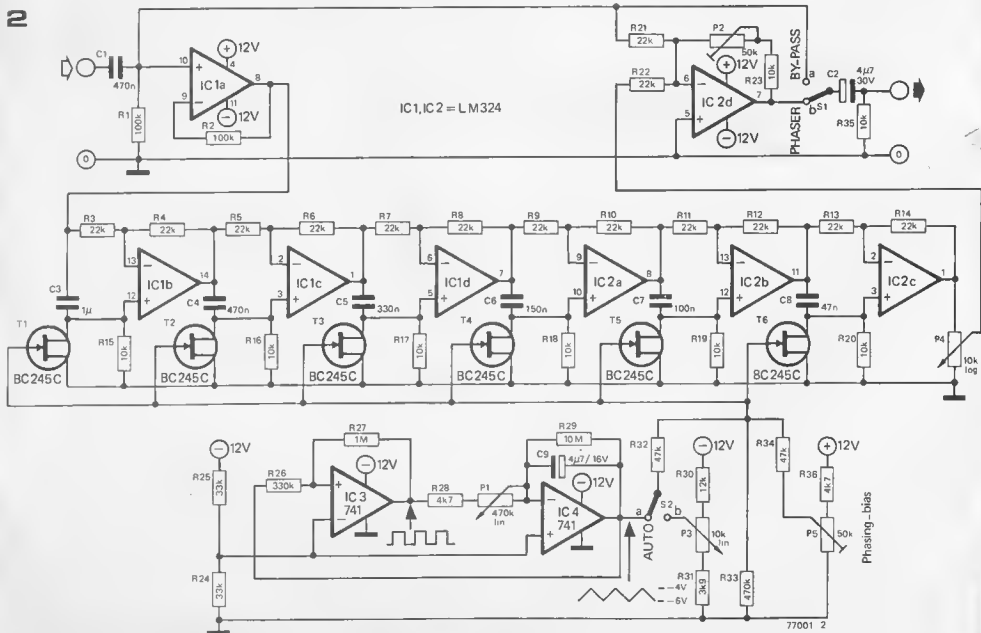
Figure 1 shows the basic circuit of a first order all-pass filter. The phase-shift is dependent on the relative values of R and C and on the input frequency. At low frequencies C has a very high impedance and the circuit simply functions as an inverting amplifier, so the phase-shift is 180° . At high frequencies the impedance of C is low and the circuit functions as a non-inverting amplifier with zero phase-shift.

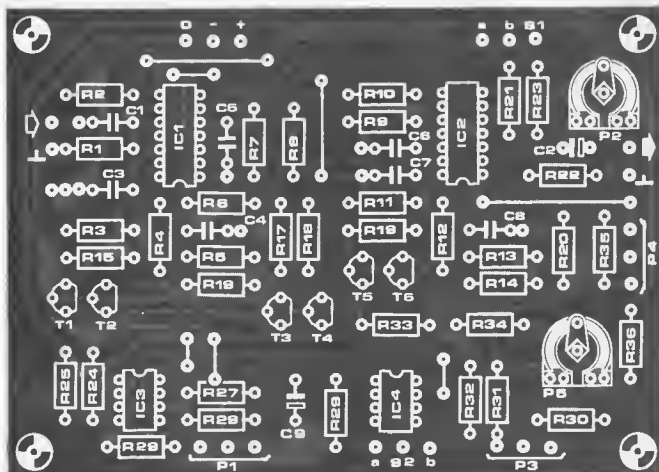
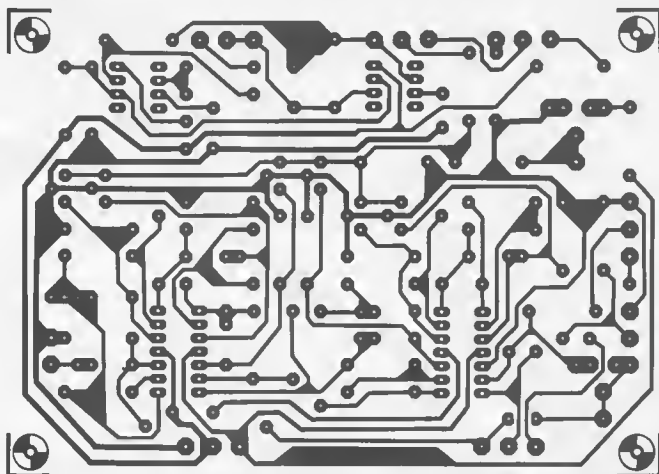
The gain of the filter depends on the relative values of R1 and R2. In this case R1 and R2 are chosen equal so that the gain is unity.



The graph shows the phase-shift v. frequency curve for the filter.

The complete circuit of a phasing unit using all-pass filters is shown in figure 2. Six all-pass filter stages are cascaded, so the total phase-shift at low frequencies can be up to 1080° ! The use of a total of ten op-amps in the circuit may seem rather excessive, but as eight of these are LM324 quad op-amps the total package count is only four ICs. IC1a functions as a unity gain input buffer.





and IC1b to IC2c are the six filter stages. The direct and phase-shifted signals are summed by IC2d. The proportion of phase-shifted signal and hence the depth of phasing can be adjusted by means of P4.

The degree of phase-shift at a particular frequency can be varied by FETs T1 to T6, which function as voltage controlled resistors. By varying the gate voltage the drain-source resistance can be increased or decreased, thus altering the effective value of 'R' in each all-pass filter and hence varying the phase-shift. This may be con-

trolled either manually by means of P3 or may be swept up and down automatically by the output of the triangular wave generator consisting of IC3 and IC4. As the gate voltage of the FETs must always be negative the output of this oscillator swings between -2 and -6 V.

The oscillator frequency may be varied by means of P1, and the best phasing effect occurs at frequencies between 0.5 Hz and 1 Hz. At higher frequencies (around 4 Hz) the phasing effect is lost but a vibrato effect is obtained instead.

The recent reduction in the price of nickel cadmium batteries has led to increasingly widespread use of these energy sources. The following circuit, which uses a 555 IC, is a simple but effective automatic charger for these popular batteries.

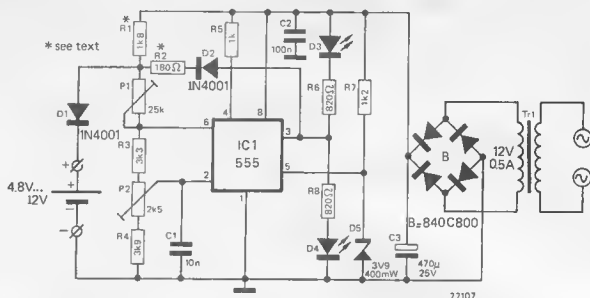
Although originally designed for normal batteries, the circuit can be adapted to charge batteries with sintered electrodes by suiting the values of R1 and R2 to the manufacturer's specifications.

To determine whether the battery is fully charged, the battery voltage is monitored. This method will only function satisfactorily

if the temperature of the battery is always the same when fully charged. For this reason D5 is placed next to the battery to provide a certain amount of automatic temperature compensation. However, if the ambient temperature varies over a wider range, then P1 should be adjusted accordingly. The IC 555 has two voltage-sensitive inputs. The input at pin 6 will switch the output to zero as soon as this input voltage exceeds the zener voltage at pin 5; the other input at pin 2 will switch the output back in as soon as this input voltage drops below half the zener voltage. Thus the voltage at which the

71

automatic charger



charger will be switched on and off can be set by means of P1 and P2 respectively. In addition, the battery is trickle-charged continuously to compensate for self-discharging.

D3 and D4 are LEDs which indicate whether the charger is on or off. The procedure for adjusting the circuit for different types of battery is as follows: the correct cut-off voltage is set by means of P1 (normally P2 will need only a single initial adjustment); the charging current is determined by R2 and the correct value for this resistor can be calculated as:

$$R2 = \frac{16 - V_{\text{batt}}}{I_{\text{charging}}}$$

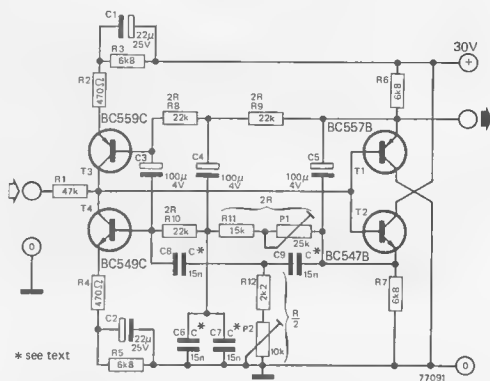
Care should be taken to ensure that the current does not exceed 200 mA, lest the IC be damaged.

The current used to continuously trickle-charge the battery is set in a similar fashion by means of R1.

The simplest way to set P1 and P2 is to use an additional variable supply. The battery is replaced by a variable supply in series with a high wattage resistor. The voltage at the cathode of D1 is then measured using a universal meter, the variable supply is set to the voltage level at which the 555 should cut off (corresponding to 'battery fully charged'), and P1 is adjusted until D3 just lights up. The variable voltage is then set at the level at which the charger should switch on, and P2 is adjusted until D4 just lights. If P2 is set incorrectly, then it is possible that the circuit will begin to oscillate.

72

complementary twin-T selective filter



This filter will pass signals at its centre frequency while attenuating signals at all other frequencies.

The input signal is fed via R1 to the bases of the complementary emitter follower T1/T2. Feedback is taken from the emitters of T1 and T2, through the twin-T network T3/T4, to the inputs of the complementary amplifier T1/T2. At frequencies removed from the centre frequency of the twin-T network, the feedback signals will pass through the twin-T unattenuated. These signals will be amplified by T3 and T4 and will appear at T3 and T4 collectors in antiphase with the input signal. The input signal, and hence the output signal from the emitters of T1 and T2, will be greatly attenuated.

At the centre frequency of the twin-T the feedback signal will be greatly attenuated, so little antiphase signal will appear at the collectors of T3 and T4 and the input signal will pass unattenuated. The output may be

taken from the emitter of either T1 or T2. The quality factor of the filter is approximately $\frac{A}{4}$, where A is the gain of the T3/T4 stage, which is $\frac{2R1}{R2}$ (R2 and R4 are equal).

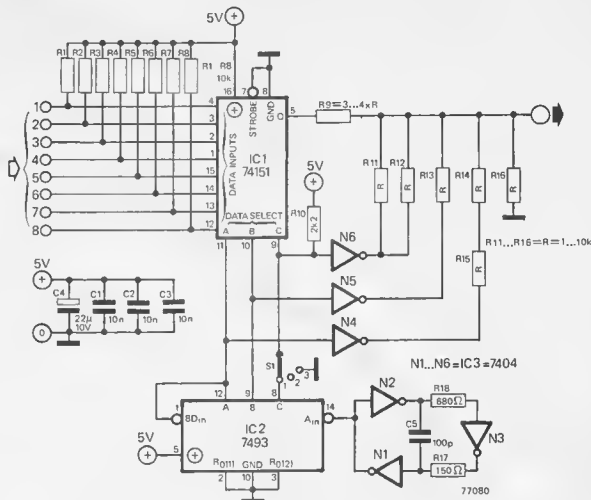
The Q-factor of this filter is thus about 500. Use of complementary stages ensures that the distortion introduced by the filters is low, which is a useful point if the filter is being used to clean up a distorted sinewave signal prior to using it for a distortion measurement.

The centre frequency of the filter is given by $f = \frac{1}{2\pi RC}$, and with the component values shown the centre frequency is about 1 kHz. P1 and P2 can be used to fine tune the filter for maximum output at the required frequency.

73

eight-channel
multiplexer

R.R. Krude, J. v. Beek

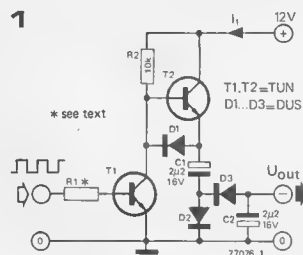


When testing logic circuits it is often necessary to examine several different pulse trains simultaneously to check that the time-relationships between them are correct. This is difficult when only a single-channel-, or at best a two-channel oscilloscope is available. Fortunately a simple eight-channel multiplexer can be constructed using only three TTL IC's. It will display up to eight pulse trains on a single-channel oscilloscope. The heart of the circuit is a 74151, one-of-eight data selector. A BCD input from 0 to 7 applied to the data select inputs allows the data on the corresponding input 1 to 8 to appear at the output. The input codes are generated sequentially by a 7493 counter which is clocked at 16 MHz by a multivibrator comprising N1 to N3. In order that the outputs should appear one above the other on the oscilloscope each output must have a different DC offset voltage added to it, otherwise the outputs would

all appear intermingled in a single trace. This offset voltage is generated by a simple D/A converter circuit consisting of N4 to N6 and R11 to R15. This generates a DC voltage proportional to the binary count of IC2, which is added to the output at the junction of R9 and R16. The value of 'R' is not critical and can be anywhere between 1 k and 10 k. However, fairly close tolerance resistors should be used (1% or 2%), otherwise the eight traces may not be uniformly spaced on the screen.

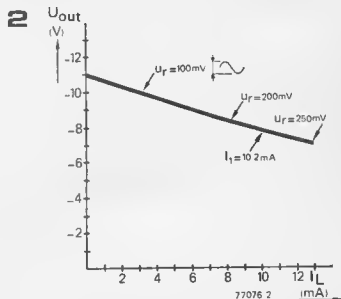
Switch S1 selects the number of channels which are displayed. In position 1 all eight channels are displayed. In position 2 the 'C' input of the multiplexer is held high by R10, so channels 5-8 are displayed. In position 3 the 'C' input is held low and channels 1-4 are displayed. The circuit can be used with input frequencies up to a few hundred kilohertz.

74

negative
supply from
positive
supply

It is sometimes necessary to provide a negative supply voltage in a circuit that otherwise uses all positive supply voltages, for example to provide a symmetrical supply for an op-amp in a circuit that is otherwise all logic ICs. Providing such a supply can be a problem, especially in battery operated equipment.

In the circuit shown here T1 is turned on and off by a squarewave signal of 50% duty-cycle at approximately 10 kHz. In logic circuits it is quite conceivable that such a signal may already be available as clock pulses. Otherwise an oscillator using two NAND gates may be constructed to provide it.

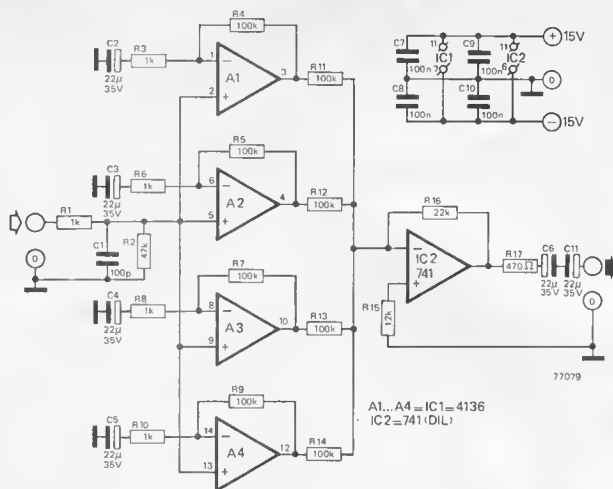


When T1 is turned off, T2 is turned on and C1 charges through T2 and D2 to about 11 V. When T1 turns on, T2 turns off and the positive end of C1 is pulled down to about +0.8 V via D1. The negative end of C1 is now about 10.2 V negative so C1 discharges through D3 into C2, thus charging it. If no current is drawn from C2 it will eventually charge to around -10 V. Of course, if a significant amount of current is drawn, the voltage across C2 will drop as shown in the graph and a 10 kHz ripple will appear on the output.

75

noise
cancelling
preamp

C. Chapman



IC operational amplifiers seem to offer an attractively simple means of building audio preamps, but unfortunately ICs generally offer inferior noise performance to the best discrete circuits. However, as quad op-amp ICs are now available at modest cost a novel solution to this problem is possible.

If a number of identical amplifiers are fed with the same signal and the outputs are summed then, since the signals and the amplifiers are the same, there will be a high degree of correlation between them, and the total output signal will simply be the algebraic sum of the individual output signals. However, since the noise voltages generated by each amplifier are random they are uncorrelated and will tend to cancel, and it can be shown that the total noise output is only the geometric sum of the individual noise voltages.

The signal-to-noise ratio of the output signal is thus improved by a factor \sqrt{n} , where n is the number of amplifiers. Thus if four amplifiers are used, the signal-to-noise ratio is doubled, i.e. increased by 6 dB. This may

not seem much of an improvement for the use of four amplifiers, but since the four amplifiers are contained in one relatively inexpensive IC the outlay in terms of money, space and constructional complexity is fairly small.

The circuit shows a practical implementation of this idea using a 4136 quad op-amp, with a 741 as the summing amplifier. The overall gain of the circuit is 100 and the output noise voltage measured over a frequency range 10 Hz to 15 kHz was $60 \mu\text{V}$, which corresponds to an input noise level of 600 nV .

The system can easily be extended to give a greater noise reduction although since the noise reduction is equal only to the square root of the number of amplifiers a law of diminishing returns applies. However, using four ICs (16 amplifiers) a noise reduction of 12 dB is possible. This probably represents the maximum which is economically feasible, as even a further 6 dB reduction would require no less than 64 amplifiers!

76

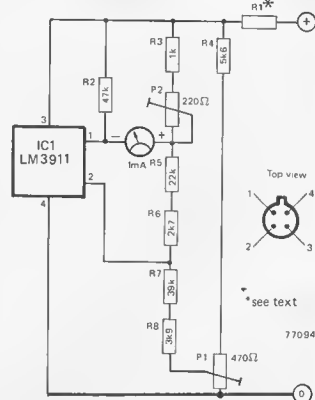
room
thermometer

Using a National LM3911 IC, a 1 mA meter and a few resistors it is a simple matter to construct a thermometer to measure over the temperature range -20° to $+50^\circ\text{C}$, which should be adequate for all but polar climates! As the circuit is intended as a room thermometer the entire circuit operates at the temperature which is being measured, so the resistors used should be low-temperature coefficient types to maintain the accuracy of the circuit.

To calibrate the thermometer the meter scale must first be marked out linearly from zero = -20° to full-scale = $+50^\circ$. With P2 set to its mid-position the circuit should be placed in a freezer or the freezing compartment of a refrigerator set to -20°C and P1 should be adjusted until the meter reads -20 . The circuit should then be placed in a temperature of $+50^\circ\text{C}$ and P2 adjusted until the meter reads 50. Of course it is also possible to mark out the scale from 0°F to 120°F and calibrate zero and full-scale accordingly.

P1 and P2 interact to a small extent, so it may be necessary to repeat the procedure several times until both the -20 and $+50$ readings are accurate.

As the IC contains its own stabiliser the

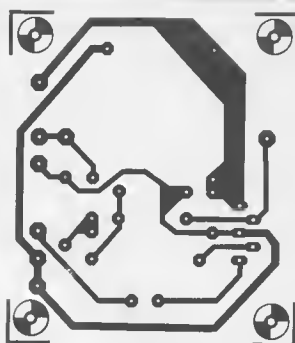
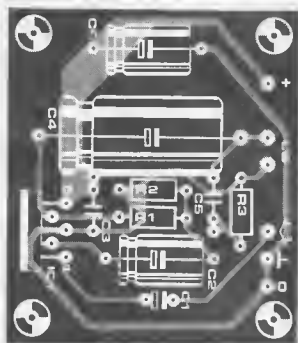


supply voltage is not critical provided the value of R_1 is chosen so that about 3 mA flows through it. The value of R_1 is given by

$$R_1 = \frac{V_b - 6}{3} \text{ (k}\Omega\text{)}.$$

77

4W car radio amplifier



EPS 77101

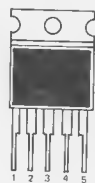
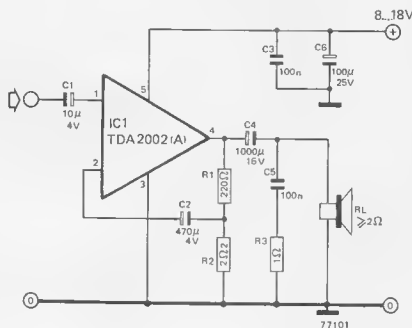
The TDA2002 and TDA2002A are integrated circuit amplifiers specially designed for use in car radios, where the adverse electrical environment places great demands upon the reliability of circuits.

The supply voltage may be anywhere between +8 and +18 V, and the IC will accept transient voltage peaks of up to 28 V without damage. The IC can supply a short-circuit output current of 3.5 A and dissipate 15 W of power at a case temperature of 90°C. At a supply voltage of 14.4 V (fully-charged battery) the maximum output power is at least 4.8 W, and typically 5.2 W, into a 4 Ω load.

The IC will, in fact, drive load impedances as low as 2 Ω, in which case the maximum output power is at least 7 W and typically 8 W. The above power figures are all measured at 10% distortion, but obviously at lower output powers the distortion is much less (typically 0.2%). In the circuit shown the gain of the amplifier is 100, determined by the ratio of R1 and R2.

The heatsink for the IC should be 45 sq. cm of 3 mm thick aluminium, or a commercial heatsink of 8°C/W (or less) thermal resistance may be used.

(SGS/Ates).



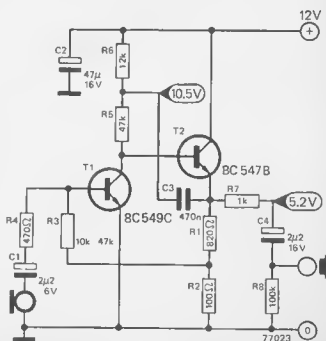
78

microphone preamp

This preamp is specifically intended for use with low impedance microphones; its advantages are high output level, large bandwidth and extremely low noise figure. The maximum gain of the preamp is approx. 200. Depending upon the sensitivity of the microphone used the gain can be adjusted by altering the value of resistor R3 (for which a suitable typical value is around 22 k).

The low noise figure (virtually undetectable in the lab) is obtained by precise impedance-matching of the input. Optimal results are therefore obtained only with microphones of 500 to 600 Ω impedance. For 200 Ω microphones R4 should be reduced in value to 220 Ω, and C1 increased to 4μ7.

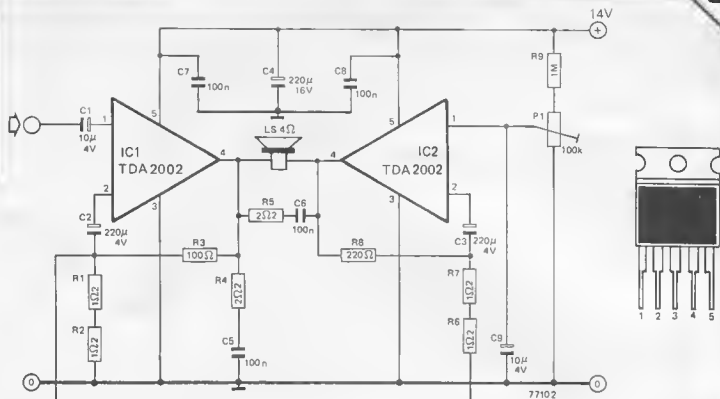
Sound 'perfectionists' may wish to use metal film resistors for R3...R6 and parallel-connected MKM capacitors in place of an electrolytic capacitor for C1. Further details: with an input signal of 3.5 mVpp and maximum gain, an output signal of 800 mVpp was obtained. The maximum



output level is approx. 10 Vpp for an input of 50 mVpp. The frequency response was flat within 3 dB from 50 Hz...100 kHz.

79

15 W bridge amplifier for car audio



When a normal capacitor-output amplifier is used in a car the output power is limited by the relatively low supply voltage of 12–14 V. With a fully-charged battery the peak-to-peak output voltage is about 14 V, the peak output voltage 7 V and the RMS output 4.9 V. This means that the maximum RMS output power into a 4 Ω load is about 6 W, assuming no losses in the amplifier output stage.

The output power can be increased by decreasing the load impedance, but this means connecting speakers in parallel, and halving the load impedance only doubles the output power. A better solution is to increase the available output voltage. Since

$$\text{power} = \frac{U^2}{R}$$
 doubling the output voltage increases the power by a factor of four.

Since it is not very practical to increase the supply voltage the simplest solution is a bridge output stage, as shown in the diagram.

As one end of the loudspeaker is no longer grounded the peak voltage across the loudspeaker can be up to 14 V (28 V peak-to-peak), so the RMS voltage is 9.9 V, which gives a theoretical maximum output of 24 W into 4 Ω. In practice, however, inevitable losses in the output stage limit the maximum power to around 15 W into 4 Ω.

The circuit uses two TDA2002 IC audio amplifiers, described elsewhere in this issue. IC1 is connected as a non-inverting amplifier, while IC2 functions as an inverting amplifier, so their outputs are antiphase. The voltage gain of the circuit is approximately 150.

P1 varies the offset voltage of the circuit and should be adjusted, under no-signal conditions (the input shorted to supply common) with the loudspeaker disconnected, until the DC voltage between the output terminals is zero.

(SGS/Ates).

80

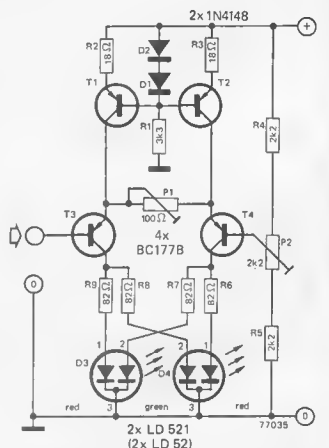
tuning indicator

This circuit is designed to replace the moving coil centre-zero meter which is used as a tuning indicator in many receivers. The circuit dispenses with the moving coil and provides rapid and accurate tuning.

The circuit employs two (unfortunately still fairly expensive) two-colour LEDs*, and operates on the principle of adjusting the tuning of the receiver until both LEDs show the same colour.

The AFC control voltage in the FM receiver is taken as the input signal**. As long as the DC-level of this signal is higher than the base voltage of T4 (set by P2), transistor T3 is turned off and T4 turned on, so that the right (e.g. green) diode of the bi-colour LED D3 and the right (e.g. red) diode of LED D4 light up. If the input voltage drops below this level, then T3 will be gradually turned on and at a certain point (adjustable by means of P2) T4 will turn off, in which case the reverse process occurs, i.e. D3 will be red and D4 green.

It is clear that between these two extreme states the LEDs will produce an in-between colour from orange to yellow. When the input voltage is exactly equal to the value preset by P2 (i.e. the circuit is on tune),



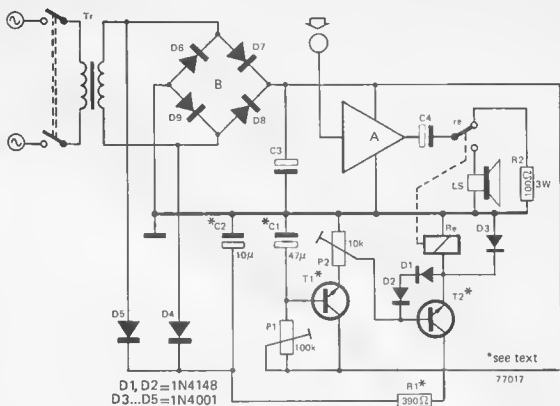
then both LEDs will show a colour midway between red and green (orange-yellow). The tuning range between the extreme states can be adjusted by means of P1.

The advantage of the circuit is that the light intensity of the LEDs will remain constant, since the current sources T1 and T2 ensure a constant current. It will therefore work over a wide range of supply voltages; the total current consumption is approx. 70 mA.

* Note that these are not the 'normal' type of two-colour LEDs where the two LEDs are connected in a reverse-parallel configuration. They should be common cathode types, such as the Knitter LD521 or LD52.

** For some suggestions, see 'LED tuner' elsewhere in this issue.

J. Rongen



The ratings of transistors T1 and T2 should be chosen to suit the amplifier supply voltage. Medium power transistors such as BC142's should be adequate in most cases.

82

voltage
controlled
monostable

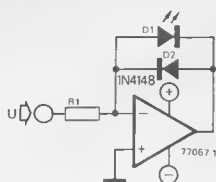
$$t \approx \frac{C \cdot V_{tr} \cdot R_2}{(V_{in} - 3.6) \cdot B}$$

C = external capacitor (max. 100 μ)

83

voltage-
controlled
LED
brightness

C. Chapman

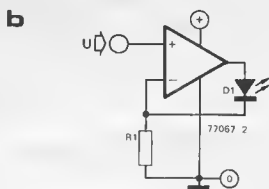


It is sometimes necessary to make the brightness of an LED vary in proportion to the magnitude of a DC control voltage, which in some cases may be less than the forward voltage drop of the LED.

The brightness of an LED is proportional to the current flowing through it, so the circuit required is a voltage/current converter which will provide a current through the LED independent of the forward voltage drop. This requirement is met by the well-known op-amp active rectifier circuit.

If a positive voltage is applied to the input in figure (a) then the output voltage will swing negative until the LED conducts. As the inverting input of the op-amp is a virtual earth point the current flowing through R_1 and hence through the LED is $\frac{U}{R_1}$. In the

absence of an input the op-amp offset could cause the output to swing positive and exceed the reverse breakdown voltage of the LED. For this reason D2 is included to



limit the maximum positive excursion to +0.6 V. Negative voltages may be used by reversing D1 and D2.

In figure (a) the input voltage must supply all the current taken by the LED, but figure (b) shows a circuit with a high input resistance that takes virtually no current from the input voltage.

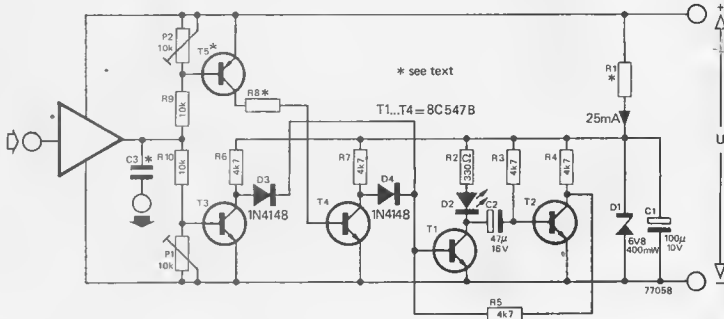
The positive input voltage is applied to the non-inverting input of the op-amp, and the output voltage of the op-amp swings positive until the voltage on the inverting input is the

same. A current $\frac{U}{R_1}$ thus flows through R_1 and since it is provided by the op-amp output it also flows through D_1 .

The value of R_1 is simply $\frac{U_{\max}}{I_{\max}}$, where

these are respectively the maximum input voltage and maximum LED current required. Any op-amp capable of supplying the required current may be used.

84

clipping
indicator

This circuit is designed to indicate the onset of clipping in an amplifier on both positive and negative peaks. Clipping occurs when the output of an amplifier swings up or down to its positive or negative limit, which is usually just below the supply voltage, so the circuit is designed to detect this.

When the amplifier output clips positive T5 will turn off, which will cause T4 to turn off, triggering the monostable T1/T2, which will cause D2 to light for about 200 ms. If the amplifier clips negative then T3 will turn off, again triggering the monostable. If the amplifier clips briefly then just a short flicker of the LED D2 will be seen, but if the amplifier clips continuously the monostable will be continuously retriggered and the LED will appear to be permanently lit. Potentiometers P1 and P2 adjust the exact level at which the indicator operates. If the amplifier clips within 0.6 V of positive or negative supply voltage then these presets may be omitted.

If the amplifier has a single (positive) supply rail and capacitor-coupled output then the

input of the circuit should be connected to the 'hot' end of this capacitor, i.e. to the top of C3 in the diagram (C3 is the output capacitor of the amplifier). The supply rails to the circuit should be connected between + supply and 0 V.

If the amplifier has a symmetrical supply and direct-coupled output then the input (junction of R9 and R10) can be connected direct to the output of the amplifier. The supply connections to the circuit should be taken between + supply and - supply.

R1, D1 and C1 provide a stabilised low-voltage supply for the circuit. R1 is calculated by the equation: $R1 = \frac{V_s - 6.8}{25}$ (k Ω).

R8 is chosen so that about 1 mA flows through it and is given by $R8 = \frac{V_s}{I}$ (k Ω)

Where V_s is the total supply voltage between + and 0 or + and - rails as appropriate. For values of V_s up to 45 V T5 may be a BC157B or BC557B and for voltages up to 65 V a BC556N.

85

car burglar alarm

R.T.G. Steenis

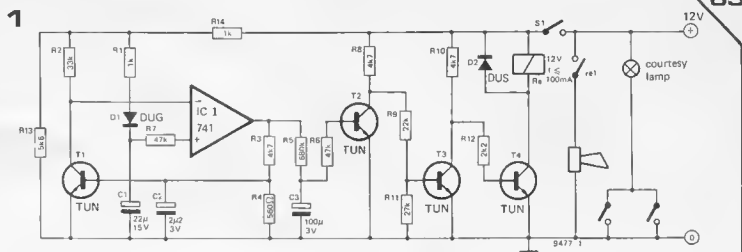


Figure 1. Complete circuit of the car burglar alarm.

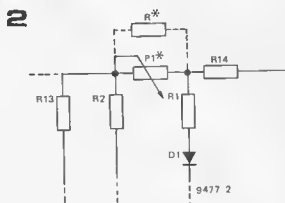
The theft of cars, and articles from cars is now a booming business. Fortunately most thieves like easy pickings, and the casual thief will tend to avoid vehicles that are securely locked with no valuables left visible. For the professional villain a more active form of deterrent is required, and this simple burglar alarm should fill the bill in most cases. It can be installed with a minimum of interference with the existing car wiring, and can be arranged to sound an alarm should a thief attempt to enter the vehicle.

The circuit operates by sensing the small voltage drop that occurs along the battery lead when a door is opened and the courtesy light draws current. The circuit offers complete protection for a two door car. For four door cars where the courtesy light operates only on the front doors it may be advisable to fit extra courtesy light switches to the rear doors. If the car boot is fitted with an interior light then it also will be protected.

The complete circuit of the alarm is given in figure 1. It is armed by closing a concealed switch S1. When this occurs the inverting input of IC1 is pulled up to about 10 V via R2. C1 charges through R1 and D1 until the non-inverting input of IC1 acquires a voltage just below that on the inverting input, due to the forward voltage drop of D1. The output of IC1 is thus at 0 V. If the battery voltage subsequently falls suddenly due to the door being opened the voltage at the inverting input will fall below that on the non-inverting input, since C1 will hold the non-inverting input voltage constant. The output of IC1 will rise to +12 V and T1 will turn on, pulling the inverting input down to 0 V so that the circuit will remain latched even if the door is subsequently closed. R3 and C2 form a lowpass filter that prevents any extraneous interference from turning on T1.

After a short delay determined by the time constant $R5 \cdot C3$ T2 will turn on, turning off T3 which will turn on T4 and energise the

Figure 2. The threshold voltage of the alarm may be decreased if the voltage drop is insufficient to trigger the alarm.



* see text

relay, sounding the horn. The delay allows the rightful owner to enter the vehicle and disarm the circuit by opening the concealed switch S1. C3 must be a low-leakage (i.e. tantalum) capacitor.

To ensure a reasonable voltage drop for reliable functioning the circuit should be connected to the +12 V line as near to the courtesy lamp as possible. It is obviously no use connecting the circuit direct to the battery terminal! If the circuit fails to function it may be necessary to lower the trigger threshold by inserting a 470 Ω potentiometer as shown in figure 2 and adjusting until the circuit operates. The resistance of the pot may then be measured and it can be replaced by a fixed resistor of the same value.

Operation

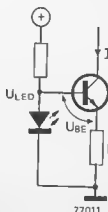
On leaving the car, open the door and then close the concealed switch. Since the door is already open the alarm will not be triggered, and the door can then be closed without triggering the alarm, which responds only to a drop in battery voltage.

Depending on type and the current flowing, the forward voltage drop of an LED may lie between 1.4 and 2 volts. The temperature coefficient of this voltage is about $-1.5 \text{ mV}/^\circ\text{C}$.

As this is virtually the same as the temperature coefficient of the base-emitter voltage of a silicon transistor, it is very easy to construct a constant current source with almost zero temperature coefficient, as shown in the accompanying circuit.

The current is approximately
$$\frac{U_{LED} - U_{BE}}{R}$$

Since the temperature coefficients of the LED and the transistor are almost the same they cancel out and the current is almost independent of temperature.



86

using LEDs as reference diodes

87

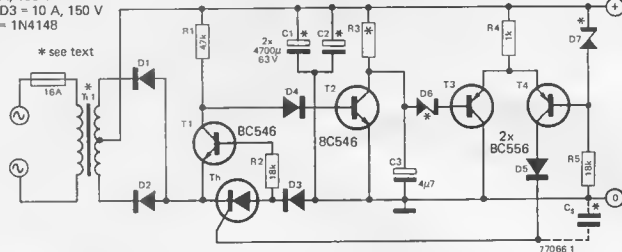
thyristor
switched
regulator

T. Hagman

Th = 6 A, 100 V
D1, D2, D3 = 10 A, 150 V
D4, D5 = 1N4148

1

* see text



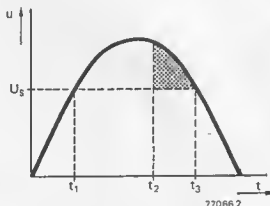
Conventional stabilised power supplies which use a series regulator transistor suffer from one serious disadvantage: a large amount of power is dissipated in the series transistor, especially when the output current is large and the difference between the input and output voltages is high. A solution to this problem is to use a thyristor switched power supply. As thyristors are either turned off (passing no current) or turned on (passing current at a low forward voltage drop) they dissipate relatively little power.

The circuit functions as follows: D1 and D2 full-wave rectify the AC supply from the secondary of the transformer. Assuming that reservoir capacitors C1 and C2 are charged to a certain voltage, then at the beginning of each half cycle of the AC waveform T1 will be turned off, since its emitter voltage will be higher than its base voltage. T2 will be turned on, shorting out C3, so T3 will be turned on and T4 turned off. When the rectified voltage exceeds the voltage on C1 and C2 by about 1.5 V T1 will turn on, turning off T2 and allowing C3 to charge through R3 until T3 turns off and T4 turns on, triggering the thyristor. C1 and C2 will now charge until the rectified voltage falls below the voltage on C1 and C2, when the thyristor will turn off and the cycle will repeat.

The time for which the thyristor is switched on is represented by t2-t3 in figure 2.

If the voltage across C1 and C2 (i.e. the output voltage) should tend to rise then the base voltage of T4 will rise by the same amount, pulled up via D7. It will thus take longer for C3 to charge to the point where the thyristor is triggered, i.e. the thyristor

2



will trigger later in the cycle and C1 and C2 will receive less charge.

Should the voltage on C1 and C2 tend to fall then the base voltage of T4 will also fall and it will take less time for C3 to charge to the point where the thyristor triggers. The thyristor will thus trigger earlier in the cycle and C1 and C2 will receive more charge.

This circuit is particularly useful as a power supply for audio amplifiers where the power requirements are fairly large and conventional regulators with large heatsinks would take up too much space. Component values are given in the table for use with the 45 and 60 V versions of the Equin amplifier described in Elektor 12 and 13, April/May 1976.

The circuit can easily be adapted to suit other supply voltages by changing the values of R3, D6, D7 and the transformer voltage. The combined capacitance of C1 and C2 should be at least 10,000 μ F.

U _s	45 V	60 V	other
R3	22 k	33 k	approx. $\frac{1}{2}$ U _s k
D6	18 V	27 V	approx. $\frac{1}{2}$ U _s V
D7	27 V	33 V	U _s - U _{D6} V

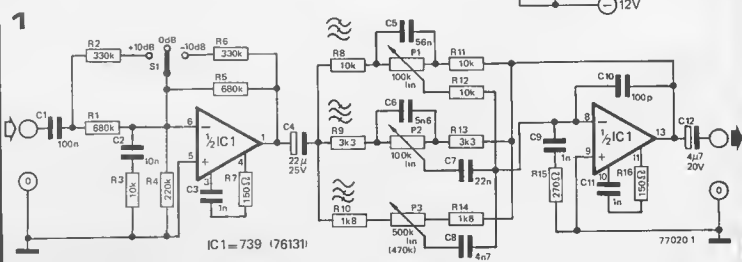
88

guitar
preamp

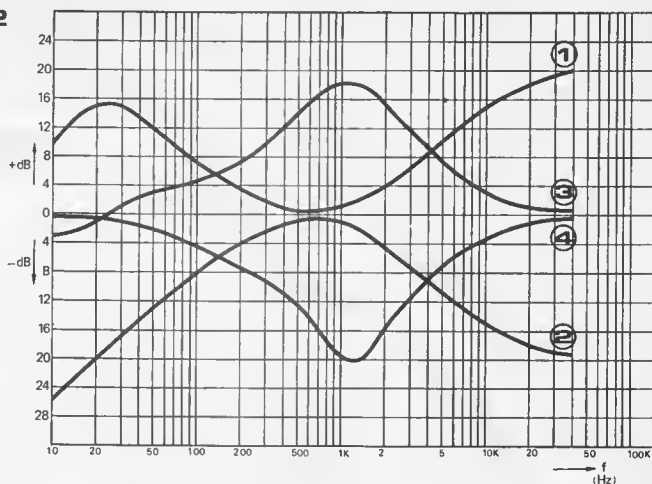
Using a μ A739 dual, low-noise op-amp it is a simple matter to construct a versatile preamplifier for a magnetic guitar pick-up. The input stage consists of an amplifier with a flat frequency response having switchable gains of -10 dB, 0 dB and +10 dB, so that it may be used with pick-ups having a variety of output levels. The switchable gain also makes possible feedback when the

guitar is brought close to the loudspeakers. This effect, much favoured by guitarists, can be achieved if the guitar amplifier power is around 20 watts or greater.

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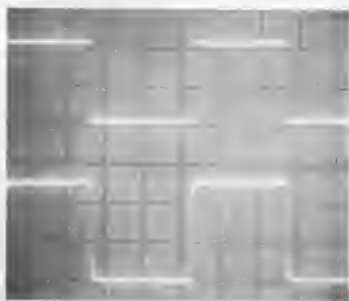
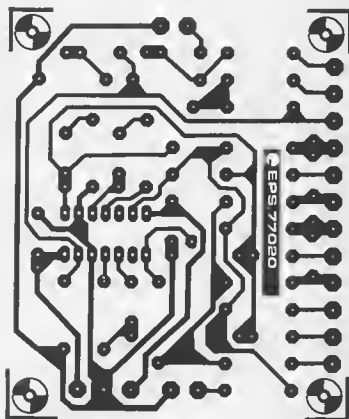
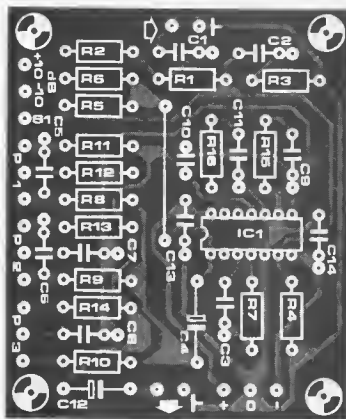


2



- ① = BASS + TREBLE BOOST, MIDDLE FLAT
- ② = BASS + TREBLE CUT, MIDDLE FLAT
- ③ = MIDDLE BOOST, BASS + TREBLE FLAT
- ④ = MIDDLE CUT, BASS + TREBLE FLAT

77020 2

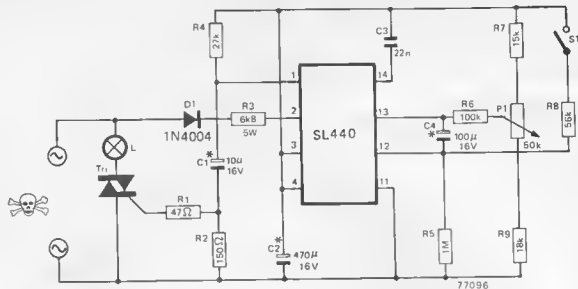


The input stage is followed by a tone control stage which possesses bass, middle and treble controls. As the frequency response of many guitar pick-ups is far from flat these controls can be used to compensate for any peaks or dips. The response of the tone control networks for different settings of the control pots is shown in the accompanying graph.

The oscillogram, the lower trace of which shows the preamp output when fed with a 1 kHz squarewave (upper trace) illustrates that the h.f. response of the preamp is fairly good. Indeed, the performance of the preamp is so good that, as well as its intended use, it may also be used in hi-fi systems.

89

fade asleep



* tantalum

Some children have less difficulty falling asleep if the bedroom light is left on. However, this means that one of the parents has to go up after half an hour or so to turn the lights off — hopefully without waking the children up again... The circuit described here will fade out the lights very slowly, either completely off or to a preset minimum (night-light) level.

As long as S1 is closed the light(s) will burn at full brightness. As soon as S1 is opened, the lights start to fade out very gradually until they reach a certain level (preset by means of P1). The fade-out time is determined by the value of C4 and by the setting of P1. As an example, if C4 = 100 µ and P1 is set at minimum it will take approximately half an hour for the lamp to fade out. If

desired, C4 can be increased; however, it is not advisable to go above about 470 µ.

The circuit *must* be mounted in a well-insulated case, and P1 should be a potentiometer with a plastic spindle.

The type of triac required will depend on the load, of course. It is advisable to select a type that is capable of handling a current of up to

$$I_L = 3 \frac{P_L}{U_M}$$

where P_L is the nominal 'wattage' of the lamp and U_M is the nominal mains voltage. A 'cold' filament draws a relatively heavy current!

(Plessey application)

90

CMOS PLL

As PLL (phase-locked loop) ICs are still somewhat expensive it seems reasonable to look around for a cheaper alternative, particularly for non-critical applications that do not require such high specifications.

Using two CMOS NAND gates it is possible to construct a CCO (current controlled oscillator) as described elsewhere in this issue. If a 4011 quad two-input NAND gate IC is used this leaves one gate to act as a phase comparator and another as an input amplifier.

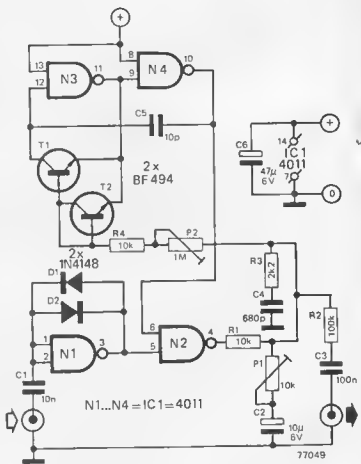
The circuit shows a complete PLL using one 4011 and a few discrete components. Considering the simplicity and low cost of the circuit the results obtained were surprisingly good, and using a typical 4011 the following measurements were taken.

CCO frequency range (adjusted by P2): 25 kHz – 800 kHz. Hold range: 20% of CCO free-running frequency. Output level: 45 mV measured at $f_{in} = 500$ kHz, deviation = ± 30 kHz, modulation frequency = 1 kHz. AM suppression for 30% AM: better than 40 dB. Minimum input level: less than 2 mV from 50 Ω source.

These measurements were taken at a supply voltage of 6 V, when the current consumption was 600 µA.

Since different IC manufacturers use different processes and different chip geometries it might be expected that results would vary when using different types of IC. The best results were obtained using ICs in which the gates had a steep transfer characteristic (better approach to an ideal switch) and lowest crosstalk between gates.

In our experience, the Solid State Scientific SCL 4011 is a good example of this type of chip.

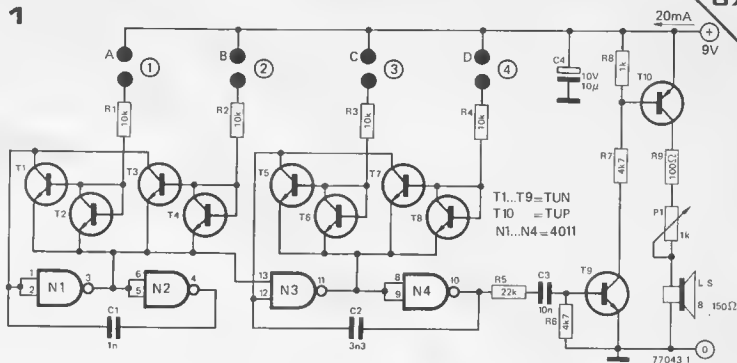


The 4011 PLL is particularly suitable for narrow-band FM demodulation, and in fact proved superior, in terms of S/N ratio and impulse noise rejection, to several monolithic PLL ICs.

91

osculometer

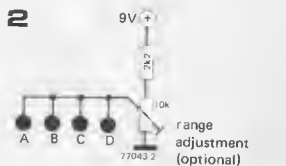
1



'Lie Detector' machines, which measure skin resistance, can provide great amusement at parties, especially if two participants each hold one electrode and indulge in some form of physical contact (e.g. kissing). The meter can then be calibrated in degrees of passion. A variation on this theme is a circuit that produces an audible output rather than a meter indication, which is even more amusing. The circuit consists of two current controlled oscillators (described elsewhere in this issue). The output of oscillator N1/N2 gates oscillator N3/N4 which produces some interesting effects. The output of N4 is used to drive an audio amplifier comprising T9 and T10.

The circuit has provision for eight electrodes for up to four pairs of participants. As the resistance between a pair of electrodes decreases then the frequency of the corre-

2



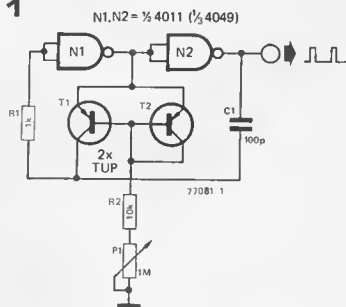
sponding oscillator will rise, so the more ardent the embrace the higher the oscillator frequency. The gating effect between the two oscillators produces some unusual sounds.

For safety reasons the circuit should be battery powered by a 9 V transistor 'power pack', such as a PP3, PP6, PP9 etc.

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CMOS CCO

1



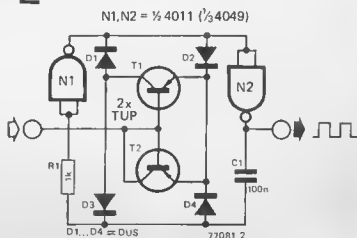
Using two CMOS NAND gates (or inverters) and two transistors it is possible to construct a simple current-controlled oscillator (CCO). The circuit of figure 1 is based on a normal two-inverter astable multivibrator. When the output of N1 is high the output of N2 will be low and C1 will charge through T1 until the threshold voltage of N1 is exceeded, when the output of N1 will go low and the output of N2 high. T1 will now operate in a reverse direction, i.e. the collector will function as the emitter and vice versa, and C1 will charge in the opposite direction. When the voltage at the collector of T1 falls below the threshold of N1, then the output of N1 will go high and the cycle will repeat. T1 and T2 form a current mirror, i.e. the collector current of T1 (which is the charging current of C1) tracks or 'mirrors'

the collector current of T2, which is, of course, controlled by the base current. If the two transistors were identical then the collector currents would be the same. A frequency range of about 4 kHz to 100 kHz is obtainable with the component values shown.

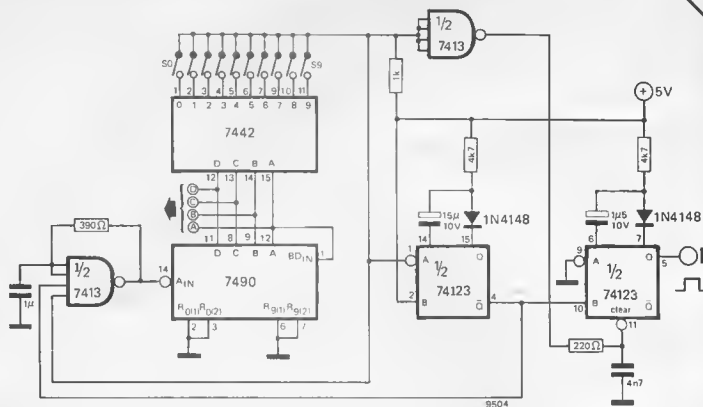
When T1 is conducting in the reverse direction T2 will be turned off and its base-emitter junction reverse-biased. If the supply voltage is greater than +5 V then this junction may break down, but as the voltages and currents involved are fairly small no damage will occur.

A circuit that avoids the unusual mode of operation of T1 and possible breakdown of T2 is given in figure 2. Here a diode bridge D1 to D4 ensures that the current through T1 and T2 always flows in the correct direction. The advantage of this circuit is that the astable may also be controlled by other asymmetric devices such as photodiodes and phototransistors.

2



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key board
decoder

When one of the keys S0...S9 is pressed the keyboard decoder generates the BCD code which corresponds to that key. To ensure that only the desired BCD information is read out the circuit also produces a strobe pulse which indicates that the information has been accessed.

The diagram illustrates how clock pulses are fed from a free running squarewave oscillator ($\frac{1}{2}$ 7413) to a decade counter (7490). The state of the counter is decoded and fed to the contact keys S0...S9. The outputs of the decoder go successively

low. Thus, the keys are scanned rapidly and sequentially until one of them is pressed. The corresponding output of the decoder will, after a certain time, go low. This '0' stops the oscillator and the counter, which then remains in the state which coincides with that of the key which has been pressed. To prevent possible mistakes arising as a result of contact bounce, the circuit includes a monostable multivibrator, which after 0.3 ms triggers a second monostable. This in turn supplies the pulse which reads in the BCD information from the 7490.

94

car headlight
alarm

R. Trost

This circuit is designed to give an audible and visible warning to the absent-minded motorist who forgets to switch off the headlamps when leaving his car.

The power supply to the circuit is taken from the headlamp switch, represented by S2. If the headlamps are switched off then the alarm obviously receives no power and does not operate. The actual light switch in the car will be more complex than S2 since it also controls the sidelights. However, examination of the car wiring diagram and a little probing with a multimeter will soon show which terminal of the switch acquires a positive voltage when the headlamps are switched on.

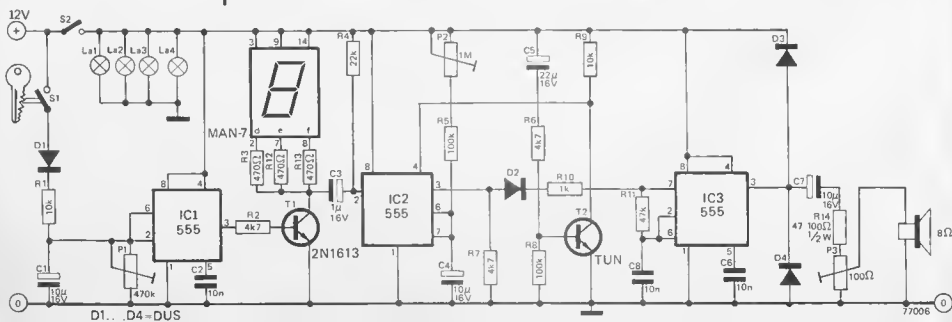
S1 represents the car ignition switch. As long as the ignition is switched on pins 2 and 6 of IC1 are pulled high via D1 and R1. When the ignition is switched off, however, this voltage will fall as C1 discharges through P1. P1 sets the time allowed for switching off the headlamps before the alarm sounds.

When the voltage on C1 falls below the trigger threshold of IC1 then, assuming the

headlamps are still switched on, the output (pin 3) of IC1 will go high, turning on T1. This lights the seven segment LED display which gives an 'L' indication. If the expense of a LED display is not thought to be justified then a single LED or lamp could be used. T1 also triggers IC2, which is connected as a monostable multivibrator. The output of IC2 goes high, thus activating astable multivibrator IC3, which begins to oscillate, producing an alarm signal from the loudspeaker.

The length of time for which the alarm sounds is determined by the period of the monostable IC2, which may be adjusted by means of P2. P3 adjusts the volume of the alarm signal.

To prevent the possibility of IC2 being spuriously triggered when the headlamps are switched on, T2 is provided. When the headlamp switch is closed C5 begins to charge through R6 and R8, which momentarily turns on T2. T2 thus holds the reset input (pin 4) of IC2 low so that it cannot trigger.



95

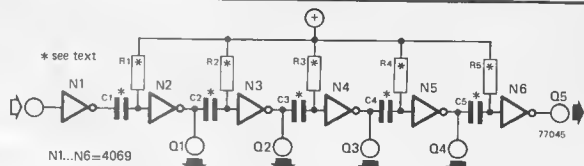
self-shifting register

A.M. Bosschaert

96

LED tuner

W. Auffermann

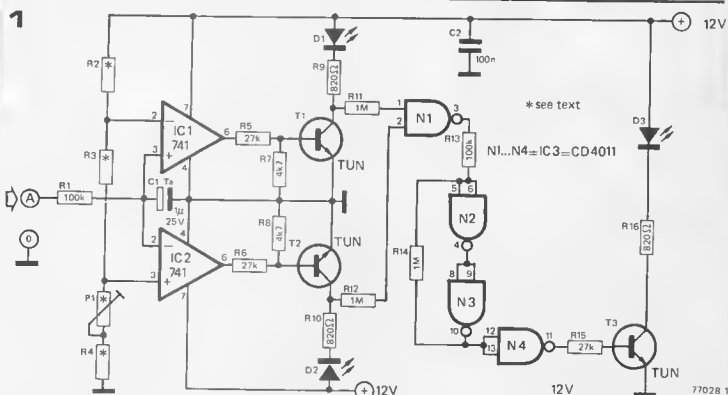


The unusual feature of this shift register is that it will transfer pulses from its input, through several stages, to the output without the need for an external clock generator. The shift speed is fixed, and is determined by the component values in the circuit.

When the input goes high, the output of N1 will go low and the input of N2 will be held low for a period determined by the time constant $R1 \cdot C1$. During this time the output of N2 will be high. When the input of N2 goes high again, the output of N2 will hold the input of N3 low for a time determined by $R2 \cdot C2$. In this way the pulse is shifted through the register. When the input

goes low, C1 will simply discharge through R1 and the output of N1, ready for the next pulse.

It is apparent that, provided the length of the input pulse is longer than the time constant $R1 \cdot C1$, the length of the output pulse is determined solely by the circuit time constants. In general the time constants $R1 \cdot C1$, $R2 \cdot C2$ etc. will all be equal, and in this case the maximum input pulse rate is determined by the fact that the interval between two pulses may not be less than the time constant $R1 \cdot C1$, otherwise pulses may overlap.

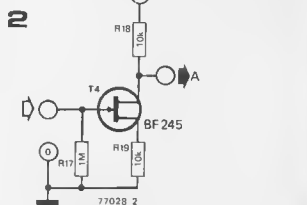


This circuit can be used as a tuning indicator, instead of the more common pointer instrument. It gives a three-LED indication of correct tuning: 'off-to-one-side', 'correctly tuned', 'off-to-the-other-side'.

A voltage is derived from the AFC control voltage in the FM receiver and fed to two comparators (IC1 and IC2). The divider chain R2, R3, P1 and R4 produces two reference voltages. If the input voltage is higher than the greater of the two reference voltages T1 will be turned on and LED D1 will light. In the other extreme case, where the input voltage is lower than the lower reference voltage, T2 will be turned on and LED D2 will light. In the in-between range, where the receiver is correctly tuned and the input voltage is somewhere between the two reference voltages, T1 and T2 will both be turned off. In this case the output of N1 will go low, the trigger circuit N2/N3 will switch, the output of N4 will go high and T3 will be turned on — lighting LED D3.

Since the AFC voltage corresponding to 'correctly tuned' varies considerably from one receiver to the next, the values of R2, R3, R4 and P1 are not given in the circuit. It is a simple matter to calculate these values for any particular application. If the total resistance is to be 20...30 k (a reasonable assumption), the voltage midway along R3 should correspond to the AFC voltage for correct tuning. To give two examples:

— assume that the 'correct' AFC voltage is 9.5 V. In this case the voltage across



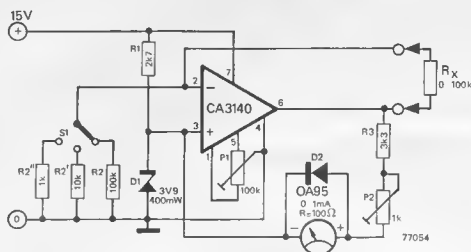
$R2 + \frac{1}{2}R3$ should equal 2.5 V and the voltage across the rest of the chain should equal 9.5 V. If R2 is selected as 4k7 and a 1 k preset is used for R3, the sum of P1 plus R4 should be approximately 20 k with P1 in the mid position. A good choice in this case would be $R4 = 18 \text{ k}$ and $P1 = 4\text{k}7$ (preset).

— assume that the correct AFC voltage is 5.6 V (as for the CA 3089!). In this case the voltage across the upper half of the divider chain should be approximately 6.5 V; reasonable values are $R2 = 12 \text{ k}$ and $R3 = 2\text{k}2$. $R4 + \frac{1}{2}P1$ should be approximately 10 k, so R4 can be 8k2 and P1 can be 4k7.

Note that R3 sets the sensitivity of the indicator, whereas P1 is used for correct calibration. Some FM detectors, notably ratio discriminators, give a 0 V output when correctly tuned. In this case the circuit shown in figure 2 can be added, between the AFC output and the input to the circuit shown in figure 1.

97

ohmmeter



Using a CA3140 FET op-amp it is easy to construct a simple, linear-scale ohmmeter. The op-amp is connected in the non-inverting mode, with the non-inverting input fed from a 3.9 V zener. The op-amp output voltage is thus given by

$$\frac{(R_X + R_2)}{R_2} \times 3.9 \text{ V.}$$

Since one end of the meter is returned to the zener the meter voltage is

$$R_X \times 3.9 + \frac{R_2}{R_2} \times 3.9 - 3.9 \text{ i.e. } \frac{R_X}{R_2} \times 3.9.$$

Since the zener voltage and R_2 are fixed the voltage measured by the meter is proportional to R_2 . The full-scale deflection of the meter is about 3.9 V, but the exact value will depend on the tolerance of the zener.

Three ranges are provided by using different values of R_2 . With $R_2 = 1 \text{ k}$ the full-scale reading of 3.9 V is obviously obtained when $R_X = 1 \text{ k}$. With R_2 equal to 10 k and 100 k full-scale readings are obtained at 10 k and 100 k. The voltmeter is simply a 1 mA meter with a nominal 3k9 series resistor, so the

0 to 1 mA scale can easily be converted to read 0 to 1 k, 0 to 10 k and 0 to 100 k. The germanium diode connected across the meter protects it in the event of an overload. To calibrate the meter it is first necessary to zero it by nulling the op-amp offset voltage. To do this P2 is first set to minimum resistance to make the meter most sensitive, and a wire link is connected across the R_X terminals. P1 is then adjusted to give a zero reading on the meter.

The meter may then be calibrated by connecting a close tolerance resistor of known value (e.g. 100 k 1%) across the R_X terminals and adjusting P2 until the meter reads correctly. To ensure good accuracy on all ranges R_2 , R_2' and R_2'' should be close tolerance types, 2% or better.

The maximum value which can be used for R_2 and hence the maximum value of R_X that can be measured depends on the input resistance of the op-amp, since any current flowing into the op-amp input will cause errors. However, with the 1.5 T Ω input resistance of the 3140 it should be possible to use values up to 10 M, assuming 10 M close tolerance resistors can be obtained.

98

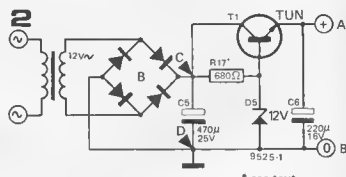
LED peak indicator

A disadvantage of the VU meters frequently used in hi-fi equipment is their inability to respond to short transients, which can lead to overrecording when used with tape recorders, and clipping when used with power amplifiers. Even many would-be peak-reading meters fail to cope with transients. Since inertia-free mechanical meters do not exist the obvious solution would seem to be a completely electronic indicator to indicate the onset of overload, and indeed many cassette recorders are now fitted with peak indicator lamps.

The circuit described here, for a stereo peak indicator, uses only one IC and a few other components.

The circuit is based on a 3900 quad Norton amplifier. Two of the amplifiers in the IC are used as comparators. Since the inputs of a Norton amplifier are current fed a resistor must be inserted in series with each input to allow them to be voltage driven. When the left channel input voltage exceeds the voltage at the slider of P1 the output of A1 will swing negative. This triggers a monostable multivibrator built around A2, which causes the LED D2 to light for a few hundred milliseconds, no matter how short the transient. In the event of a continuous overload the monostable will be retriggered continuously and the LED will appear to be continuously lit. The circuit of the right channel, comprising A3 and A4, operates in exactly the same fashion. A suitable power supply for the circuit is given in figure 2.

Figure 3 shows a printed circuit board and component layout for the indicator. The bridge rectifier for the power supply is not mounted on the board since, if the indicator is built into a piece of existing equipment it is quite likely that a suitable unregulated DC



* see text

supply may already be available. P1 and P2 are simply connected direct to the positive supply line of the equipment.

If the indicator is to be used with a tape recorder then calibration is quite simple. With the tape deck set to record a 1 kHz signal can be fed in and the record level adjusted until the record level meters move into the red. P1 and P2 may then be adjusted until D2 and D4 just light.

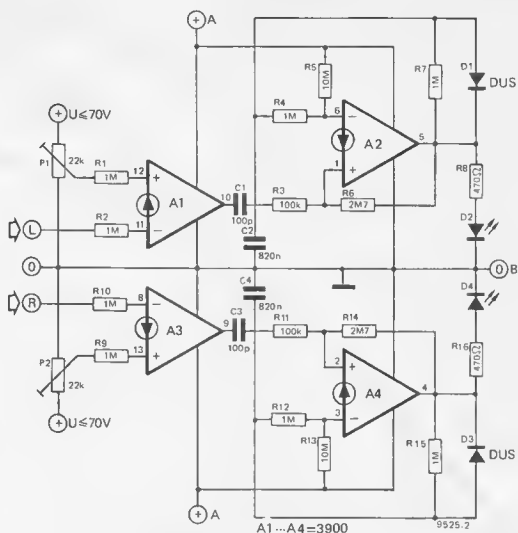
If the indicator is to be used with a power amplifier then it can be calibrated in several ways. If an oscillator and oscilloscope are available the amplifier can be fed with a 1 kHz signal which is adjusted so that the output of the amplifier is just below the onset of clipping. P1 and P2 can then be adjusted until D2 and D4 light.

If no test gear is available then the peak output voltage of the amplifier may be calculated from the equation

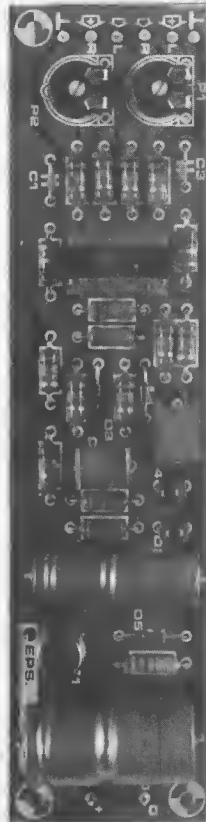
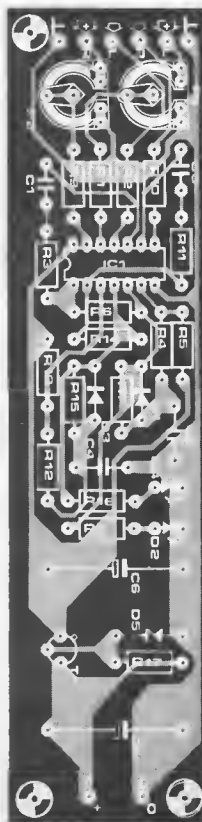
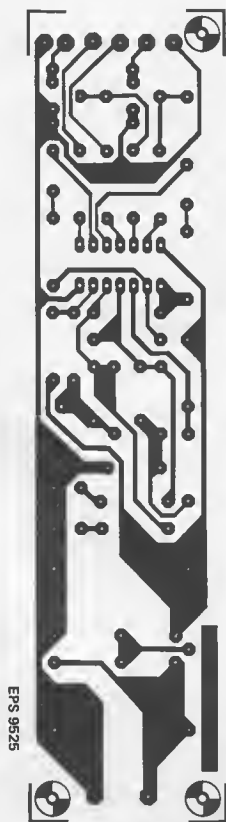
$$V_{\text{peak}} = \sqrt{2WR}$$

where W is the amplifier output power and R is the specified load impedance. The slider voltage of P1 and P2 can then be adjusted to just below this value, using a multimeter of not less than 20,000 Ω/V .

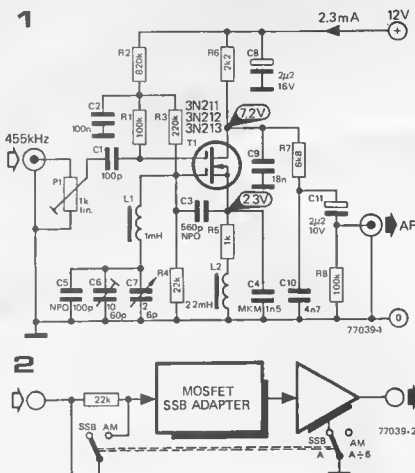
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3



99

MOSFET
SSB-adapter

In order to receive an SSB signal it is first necessary to recombine the carrier wave (which was suppressed in the transmitter) with the SSB signal. The simplest way of doing this is to feed an oscillator signal to the diode detector in the receiver. However a much better solution is to use a separate demodulator for SSB signals. The diagram shows a design for a demodulator which will adapt any shortwave receiver with an intermediate frequency of 455 kHz for SSB reception.

The advantage of a dual-gate MOSFET is that it can function simultaneously as a demodulator and an oscillator. Such a circuit is in effect a self-oscillating mixer stage, with the difference that the i.f. output signal has the same frequency as the oscillator signal. As is usual with 'direct conversion' (i.e. oscillator and input signal have the same frequency), there is the danger that the oscillator will be pulled off frequency by the input signal (forced resonance). With most dual-gate MOSFETs however, this sort of back-coupling is reduced to negligible

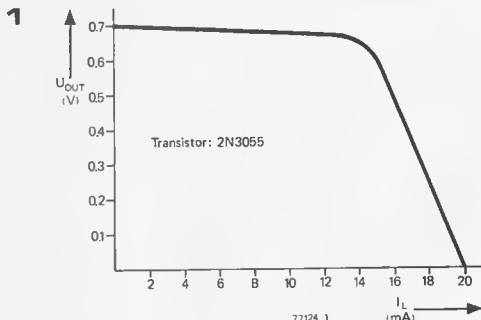
proportions. On the other hand it is also possible to take advantage of this effect and (as is the case here) construct an SSB-demodulator which can also be used as a synchronous demodulator for AM.

As is apparent from the diagram, the lower section (gate 1 and source) of the MOSFET is connected as a Clapp-oscillator with a frequency of 455 kHz; the upper section functions as a mixer stage for the oscillator and input signals. The optimum input level for SSB is approx. 15 mVpp, when the output level is 10 mVpp. For synchronous AM detection the input level has a value of 300 mVpp, and with 30% modulation the value of the output signal is approx. 60 mVpp. The circuit can be switched from AM to SSB as indicated in the block diagram. The adapter consumes approx. 2.3 mA from a 12 V supply. The supply voltage dependence of the oscillator frequency is approx. 35 Hz/volt. The synchronous range for AM is approx. 1 kHz. The measurement points shown in the diagram facilitate adjustment procedures.

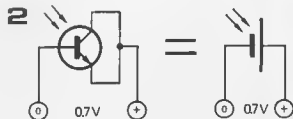
100

transistor
solar cell

H. Januschkowetz



Most amateur constructors will have one or two burnt out power transistors lying about in their junk box. If at least one of the junctions is still intact, the transistor can be converted to a solar cell by filing or sawing off the top of the case to expose the chip. In strong sunlight a 2N3055, for example, will generate about 0.7 V at currents of up



to 20 mA. The graph shows output voltage plotted against load current. As the area of the silicon chip is small compared to a normal solar cell a magnifying glass may be used to focus light onto the junction and so increase the output current. However, this is not to be recommended in very strong sunlight or the junction may be destroyed! If a good transistor is used then the output current may be doubled by connecting the collector-base and emitter-base junction in parallel, as shown in the diagram. This should not be done with faulty transistors, however, since if the faulty junction is short-circuit it would short the output of the solar cell.

Warning: It is not advisable to use old Germanium power transistors, since these may contain highly poisonous substances. However, a major semiconductor manufacturer has assured us that the more modern silicon devices, such as the 2N3055, are completely safe.



101

multiple voltage supply

Many circuits using, for example, both op-amps and logic circuits, require more than one supply voltage. The circuit described here is designed to supply four voltages of +12, +5, -7 and -12 volts, with a maximum current of 50, 300, 50 and again 50 mA respectively.

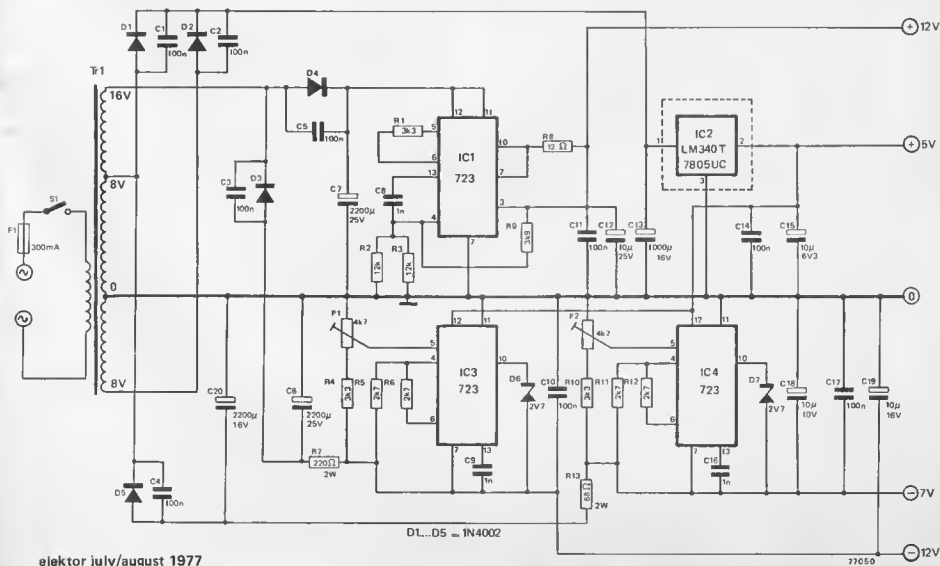
The positive supply voltages are produced in the normal fashion, using positive voltage regulator ICs; for the negative voltages it would be possible to use the special ICs which have been designed for this purpose, however these are both fairly expensive and often difficult to obtain. For this reason an alternative solution was sought. Although the 723 was designed for positive voltages, it can also be adapted for negative output voltages if, instead of being used as a series-regulator, it is connected as a shunt stabiliser (IC3 and IC4).

Shunt stabilisers suffer from the disadvantage that a constant power is taken from the mains transformer, irrespective of whether they are feeding a load. This

means that this type of circuit is not particularly efficient; however in this case, where the maximum current is only 50 mA, the power loss is negligible.

The negative output voltages can be adjusted by means of P1 and P2. After adjustment, the series-connected potentiometer and resistor can be replaced by two series-connected resistors. All the voltages supplied by the circuit are short-circuit proof; that is to say that shorting the outputs will not damage the supply. The positive outputs are provided with the usual current limiting. In the case of the shunt regulators for the negative voltages, the short-circuit current is determined by the dropper resistors R7 and R13. These should be rated at 2 W (or more) to prevent overheating.

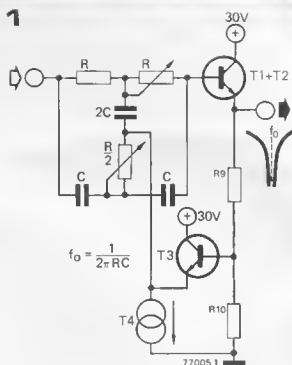
Note that it will not always be necessary to use such a complicated transformer (8-0-8-16 V). If the 5 V supply does not have to deliver much current, a 0-8-16 V (i.e. an 8-0-8 V) transformer can be used. D2 and C2 are omitted in this case.



The standard method of measuring the harmonic distortion of an amplifier is to feed the amplifier with a pure sinewave signal and to feed the distorted signal from the amplifier output into a notch filter which rejects the fundamental, leaving only the harmonic distortion products introduced by the amplifier, which can then be measured or examined on an oscilloscope.

A twin-T network tuned to the fundamental frequency of the signal will provide a very large degree of attenuation of the fundamental. However, since the Q-factor of a twin-T network is fairly low the harmonics, in particular the second, will also be attenuated, giving a too optimistic picture of the distortion.

A solution to this problem is to include the twin-T network in an active filter arrangement as shown in figure 1. Instead of connecting point A to ground in the normal



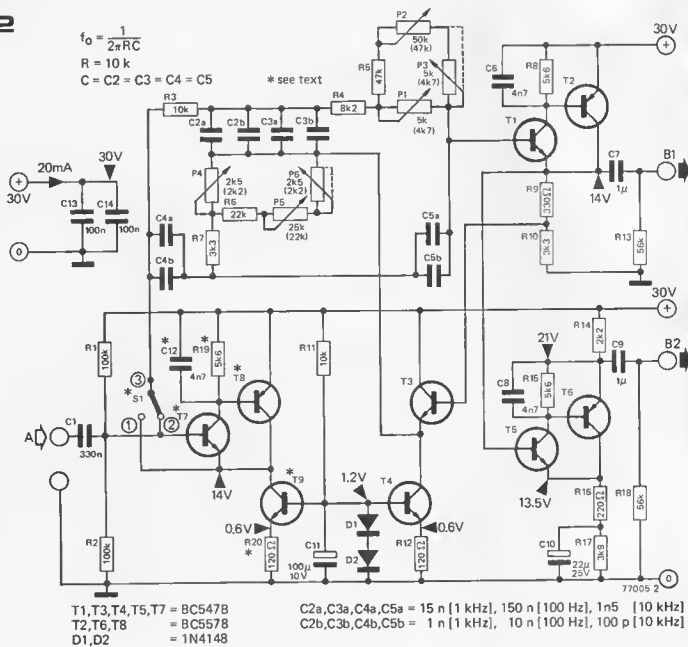
2

$$f_0 = \frac{1}{2\pi RC}$$

$$R = 10k$$

$$C = C2 = C3 = C4 = C5$$

* see text



fashion, bootstrapping is applied via emitter follower T3. This increases the Q of the network by a factor $\frac{R_{10}}{R_9}$, which virtually eliminates attenuation of the second and other harmonics.

The complete circuit of a distortion filter using this principle is given in figure 2. The twin-T network consists of resistors R3 to R7, capacitors C2a to C5b and potentiometers P1 to P6, which allow fine tuning of the filter. The filter is not designed to be tuned over the entire audio spectrum since it is intended mainly for check distortion at spot frequencies of 100 Hz, 1 kHz and 10 kHz. To this end capacitors C2a to C5b are mounted on a plug-in module so that they can easily be changed. Capacitor values for frequencies of 100 Hz, 1 kHz and 10 kHz are given, but values for other frequencies can easily be calculated from the equation:

$$f_0 = \frac{1}{2\pi RC}$$

$$\text{i.e. } C = \frac{1}{2\pi f_0 R}$$

The nominal value of R is 10 k, and the equation gives the combined value of C4a/C4b which equals C5a/C5b. The combined value of C2a to C3b is twice this. The potentiometers are used for fine tuning the filter and give a frequency adjustment of about $\pm 10\%$.

For distortion measurements on low impedance sources such as power amplifiers the signal can be fed direct to the twin-T network with S1 in position 2. The input impedance of the twin-T network at f_0 is about 7 k. For measurements on circuits with a high output impedance a 'super emitter-follower' buffer stage T7/T8 is provided. T9 is a constant current emitter

load for this stage. If this facility is not required then T7 to T9, R19, R20 and C12 may be omitted.

The output of the twin-T network is fed to a second super emitter-follower stage T1/T2. Bootstrapping from the junction of R9 and R10 is applied to the twin-T network by T3. The distortion signal is available at output B1 and also, amplified ten times, at output B2.

To use the distortion meter the amplifier to be tested is fed with a low distortion sine-wave signal at the required frequency. With the filter out of circuit the amplifier output is monitored on a 'scope' and the signal level is adjusted to give a suitable output from the amplifier. With all the potentiometers in their mid-positions the filter is switched in and the signal frequency adjusted slightly to give the minimum signal at output B1. The potentiometers can then be adjusted to null out the fundamental still more until no further reduction can be obtained.

The peak value of the distortion is then given by

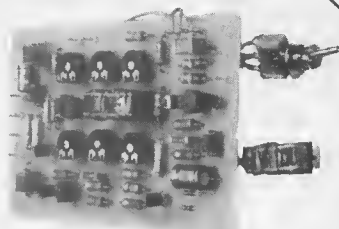
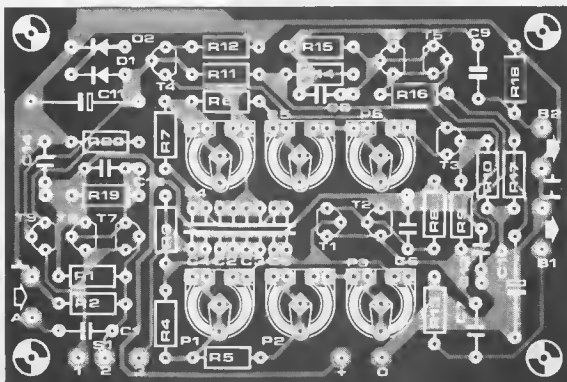
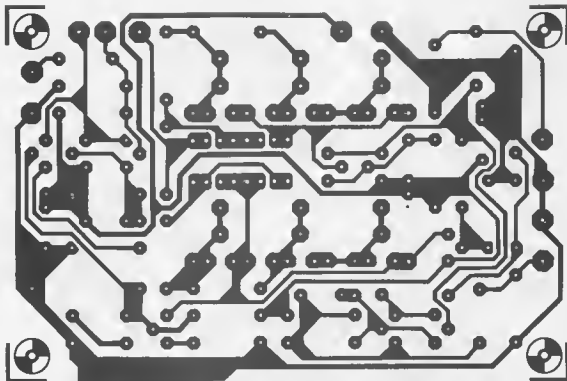
$$\frac{V_{out\ p-p}}{V_{in\ p-p}} \times 100\%$$

If the scope is not sufficiently sensitive to measure the distortion using the B1 output then the B2 output may be used. In this case the distortion is given by

$$\frac{V_{out\ p-p}}{V_{in\ p-p}} \times 10\%$$

However, during the initial adjustment stages

3



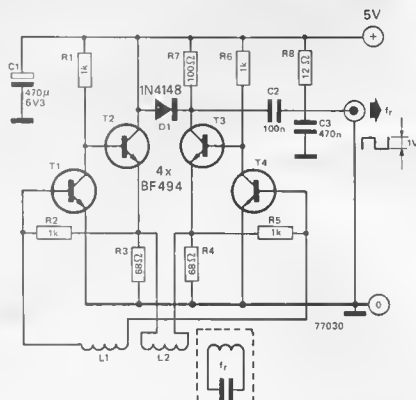
where a large proportion of the fundamental is present, the B1 output should be used as the B2 output will probably be driven into clipping.

If two distortion filters are cascaded then it is possible to measure distortion figures as low as .005%. By slightly offsetting the null frequencies of the two filters it is also possible to obtain a wider notch so that the effect of oscillator frequency drift is not so troublesome. In this case, if the B2 output of the second filter is used the percentage distortion will be given by

$$\frac{V_{out\ p-p}}{V_{in\ p-p}} \times 1\%$$

A printed circuit board and component layout for the filter are given in figure 3 (EPS 77005). Capacitors C2a to C5b are mounted on a dual-in-line component module that plugs into a DIL socket on the board.

103

LC resonance
meter

This circuit is intended to perform the same function as a conventional grid-dip meter i.e. measurement of the resonant frequency of LC-tuned circuits. Unlike a normal grid-dip meter it is not, in itself, a complete instrument, but can be used in conjunction with a frequency counter to give a direct reading of resonant frequency.

The circuit consists of a difference amplifier comprising T1 to T4 and a pair of coils L1 and L2. These coils are wound on the same former but are spaced apart so that, when the circuit is not coupled to an LC circuit,

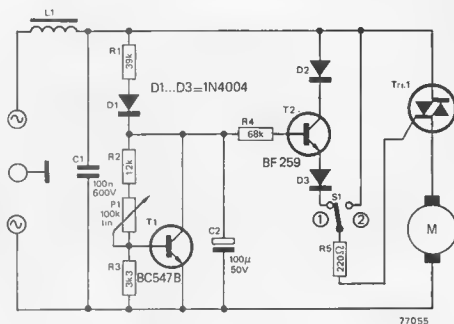
no spontaneous oscillation occurs. When the coils are brought close to an LC circuit then oscillation will occur at the resonant frequency of the LC circuit, and this frequency can be measured by feeding the collector signal of T3 to a frequency counter. No direct connection to the LC circuit is required.

It must be stressed that this is a design idea that has not been fully developed but is printed here for the benefit of the experimenter. In consequence no constructional details are given for L1 and L2.

104

drill speed
control

J. Becela



Most drill speed controllers suffer from one or more drawbacks. These include poor speed stability, excessive instability at low speeds, and high power dissipation in the series resistor used to sense motor current. The circuit described here suffers from none of these drawbacks, and in addition is extremely simple.

The mains input is rectified by D1 and dropped by R1. The current drawn by T1 can be controlled by means of P1, thus also controlling the DC voltage that appears across C2, and hence at the base of T2. T2 is connected as an emitter follower, and the voltage appearing at the cathode of D3 is about 1.5 V less than the base voltage of T2. Assuming that the motor is turning but that the triac is turned off, the back e.m.f. generated by the motor will appear at the T1 pin of the triac. So long as this voltage exceeds the cathode voltage of D3 the triac will remain turned off, but as the motor slows down this voltage will fall and the triac

will trigger. If the load on the motor increases, thus tending to slow it down, the back e.m.f. will fall more quickly and the triac will trigger sooner, thus bringing the motor back up to speed.

Since the triac can be triggered only on positive half-cycles of the mains waveform the controller will not vary the motor speed continuously from zero to full speed, and for normal full-speed running S1 is included, which turns the triac on permanently. However, the circuit exhibits good speed control characteristics over the important low speed range.

L1 and C1 provide suppression of r.f. interference generated by the triac. L1 can be a commercially available r.f. suppression choke of a few microhenries inductance. The current rating of L1 should be from two to four amps, depending on the current rating of the drill motor. Almost any 600 V 6 A triac can be used in the circuit.

Using the 3½-digit-A/D-converter LD 110/111 and a minimum of external components, it is possible to construct a universal digital voltmeter. The accuracy of the meter is approx. $0.05\% + 1$ digit. The scale of the meter runs from $-2\text{ V} \dots +2\text{ V}$ and by means of additional voltage dividers can be extended as required.

The polarity of the measured voltage is indicated by the sign in front of the highest digit. When the range of the meter is exceeded all 7 segments will flash on and off (over-range indication). If no voltage is present at the input then the meter automatically indicates 0 V (auto-zeroing). The circuit board is designed for use with Hewlett-Packard 7-segment displays 5082-7730/5082-7732 or 5082-7750/5082-7752, although other pin-compatible common-anode displays may also be used.

The input resistance of the circuit is greater than $1\text{ M}\Omega$, and the input current is approx. 4 pA .

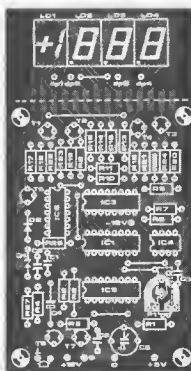
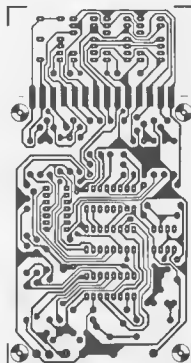
The reference voltage is produced by the FET-constant current source T6 and a transistor which is reverse biased and used as a zener diode*.

Construction and calibration

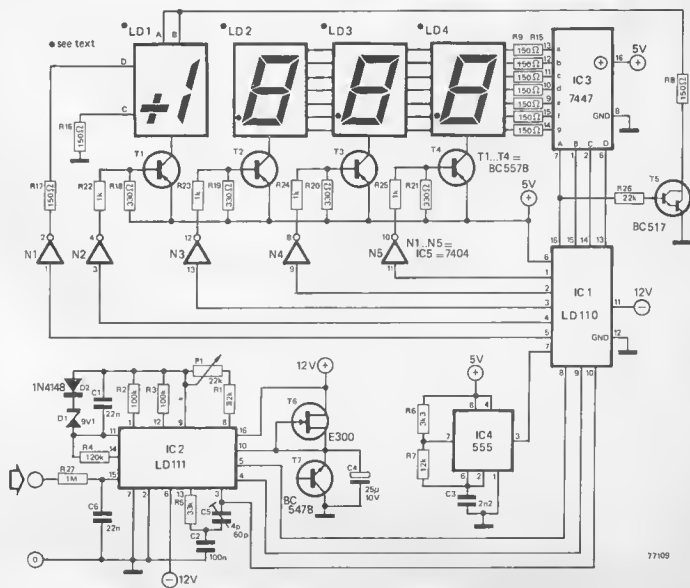
It is recommended that the meter is used with a stabilised voltage supply. A cermet trimmer should be used for potentiometer P1. After applying the supply voltage, the input should be short-circuited. Zero adjustment is then carried out using trimmer capacitor C5. Finally the meter is calibrated by means of P1 against a standard voltage. The decimal points of the displays are brought out separately. It should be noted that the series resistors in the cathode connections are not shown on the printed circuit board and should be added as required.

(Siliconix Application)

*Note that for optimum performance T6 and T7 ought to be selected types. A simpler solution is to use a $1\text{ k}\Omega$ resistor instead of T6 and a $5\text{ V}6$ voltage reference diode instead of T7.



Owing to space limitations, the p.c. board (EPs 77109) and component layout are reproduced here reduced to 50% of the original size.



TUP TUN DUG DUS

	type	U_{ce0} max	I_c max	h_{fe} min.	P_{tot} max	f_T min.
TUN TUP	NPN PNP	20 V 20 V	100 mA 100 mA	100 100	100 mW 100 mW	100 MHz 100 MHz

Table 1a. Minimum specifications for TUP and TUN.

	type	U_R max	I_F max	I_R max	P_{tot} max	C_D max
DUS DUG	Si Ge	25 V 20 V	100 mA 35 mA	1 μ A 100 μ A	250 mW 250 mW	5 pF 10 pF

Table 2. Various transistor types that meet the TUP specifications.

TUN		
BC 107	BC 208	BC 384
BC 108	BC 209	BC 407
BC 109	BC 237	BC 408
BC 147	BC 238	BC 409
BC 148	BC 239	BC 413
BC 149	BC 317	BC 414
BC 171	BC 318	BC 547
BC 172	BC 319	BC 548
BC 173	BC 347	BC 549
BC 182	BC 348	BC 582
BC 183	BC 349	BC 583
BC 184	BC 382	BC 584
BC 207	BC 383	

Table 3. Various transistor types that meet the TUP specifications.

TUP		
BC 157	BC 253	BC 352
BC 158	BC 261	BC 415
BC 177	BC 262	BC 416
BC 178	BC 263	BC 417
BC 204	BC 307	BC 418
BC 205	BC 308	BC 419
BC 206	BC 309	BC 512
BC 212	BC 320	BC 513
BC 213	BC 321	BC 514
BC 214	BC 322	BC 557
BC 251	BC 350	BC 558
BC 252	BC 351	BC 559

Table 1b. Minimum specifications for DUS and DUG.

Table 4. Various diodes that meet the DUS or DUG specifications.

DUS		DUG
BA 127	BA 318	OA 85
BA 217	BAX 13	OA 91
BA 218	BAY 61	OA 95
BA 221	1N914	AA 116
BA 222	1N4148	
BA 317		

Table 5. Minimum specifications for the BC107, -108, -109 and BC177, -178, -179 families (according to the Pro-Electron standard). Note that the BC179 does not necessarily meet the TUP specification ($I_{c,max} = 50$ mA).

	NPN	PNP
	BC 107 BC 108 BC 109	BC 177 BC 178 BC 179
V_{ce0} max	45 V 20 V 20 V	45 V 25 V 20 V
V_{eb0} max	6 V 5 V 5 V	5 V 5 V 5 V
I_c max	100 mA 100 mA 100 mA	100 mA 100 mA 50 mA
$P_{tot.}$ max	300 mW 300 mW 300 mW	300 mW 300 mW 300 mW
f_T min.	150 MHz 150 MHz 150 MHz	130 MHz 130 MHz 130 MHz
F max	10 dB 10 dB 4 dB	10 dB 10 dB 4 dB

The letters after the type number denote the current gain:

- A: α' (β , h_{fe}) = 125-260
 B: α' = 240-500
 C: α' = 450-900.

Wherever possible in Elektor circuits, transistors and diodes are simply marked 'TUP' (Transistor, Universal PNP), 'TUN' (Transistor, Universal NPN), 'DUG' (Diode, Universal Germanium) or 'DUS' (Diode, Universal Silicon). This indicates that a large group of similar devices can be used, provided they meet the minimum specifications listed in tables 1a and 1b.

For further information, see the article 'TUP-TUN-DUG-DUS' in Elektor 1, p. 9.

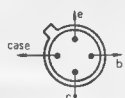
Table 6. Various equivalents for the BC107, -108, ... families. The data are those given by the Pro-Electron standard; individual manufacturers will sometimes give better specifications for their own products.

NPN	PNP	Case	Remarks
BC 107 BC 108 BC 109	BC 177 BC 178 BC 179		
BC 147 BC 148 BC 149	BC 157 BC 158 BC 159		$P_{max} = 250$ mW
BC 207 BC 208 BC 209	BC 204 BC 205 BC 206		
BC 237 BC 238 BC 239	BC 307 BC 308 BC 309		
BC 317 BC 318 BC 319	BC 320 BC 321 BC 322		$I_{c,max} = 150$ mA
BC 347 BC 348 BC 349	BC 350 BC 351 BC 352		
BC 407 BC 408 BC 409	BC 417 BC 418 BC 419		$P_{max} = 250$ mW
BC 547 BC 548 BC 549	BC 557 BC 558 BC 559		$P_{max} = 500$ mW
BC 167 BC 168 BC 169	BC 257 BC 258 BC 259		169/259 $I_{c,max} = 50$ mA
BC 171 BC 172 BC 173	BC 251 BC 252 BC 253		251...253 low noise
BC 182 BC 183 BC 184	BC 212 BC 213 BC 214		$I_{c,max} = 200$ mA
BC 582 BC 583 BC 584	BC 512 BC 513 BC 514		$I_{c,max} = 200$ mA
BC 414 BC 414 BC 414	BC 416 BC 416 BC 416		low noise
BC 413 BC 413	BC 415 BC 415		low noise
BC 382 BC 383 BC 384			
BC 437 BC 438 BC 439			$P_{max} = 220$ mW
BC 467 BC 468 BC 469			$P_{max} = 220$ mW
	BC 261 BC 262 BC 263		low noise

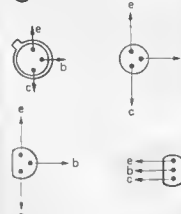
TUP TUN DUG DUS

Type	PNP = P NPN = N	VCE0 (Volt)	IC(max) (mA)	Pmax (mW) not cooled: cooled:	hFE (min)	case nr.	comments
		0 = < 20 000 = 25-40 0000 = 45-60 00000 = 65-80 000000 = > 85	0 = < 50 00 = 55-100 000 = 105-400 0000 = 405-2 A 000000 = > 2 A	0 = < 300 0 = 305-1000 000 = 1-10 W 0000 = 10-35 W 000000 = > 40 W	0 = < 20 00 = 25-50 000 = 55-120 0000 = > 125		
TUN	N	0	00	0	000		
TUP	P	0	00	0	000		
AC126	P	0	00	00	0000	2	
AF239	P	0	0	0	0	1	grounded base: f _T = 700 MHz
BC107	N	0000	00	0	000	2	
BC108	N	0	00	0	000	2	
BC109	N	0	00	0	0000	2	low noise
BC140	N	00	0000	000	00	2	
BC141	N	0000	0000	000	00	2	
BC160	P	00	0000	000	00	2	
BC161	P	000	0000	000	00	2	
BC182	N	000	000	0	0000	2	
BC212	P	000	000	0	000	2	
BC546	N	0000	00	00	0000	2	
BC556	P	00000	00	00	000	2	
BD106	N	00	000000	00000	0	7	
BD130	N	000	00000	00000	0	7	
BD132	P	000	000000	00000	0	9	
BD137	N	000	0000	0000	00	9	
BD138	P	000	0000	0000	00	9	
BD139	N	00000	0000	000	00	9	
BD140	P	00000	0000	000	00	9	
BDY20	N	000	00000	00000	0	7	
BF180	N	0	0	0	0	12	
BF185	N	0	0	0	000	10	
BF194	N	0	0	0	000	10	
BF195	N	0	0	0	000	10	
BF199	N	00	0	0	000	11	
BF200	N	00	0	0	00	1	
BF254	N	00	0	0	000	11	
BF257	P	00000	00	00	00	2	
BF494	N	0	0	0	000	11	
BFX34	N	000	00000	00	00	2	
BFX68	N	0	0	0	00	1	
BFY90	N	0	0	0	0	1	
BSX19	N	0	0000	0	000	2	
BSX20	N	0	0000	0	000	2	
BSX61	N	000	00000	00	000	2	
HEP51	P	00	0000	00	000	1	
HEP52	N	0	00	00	000	1	
HEP56	N	0	00	00	000	5	
MJE171	P	000	00000	0000	00	9	
MJE180	N	00	00000	0000	00	9	
MJE181	N	000	00000	0000	00	9	
MJE340	N	00000	00000	0000	00	9	
MPS A05	N	000	0000	00	00	13	
MPS A06	N	00000	0000	00	00	13	
MPS A09	N	00000	0	00	000	13	
MPS A10	N	00	00	00	00	13	
MPS A13	N	00	000	00	0000	13	
MPS A16	N	00	00	00	0000	13	
MPS A17	N	00	00	00	0000	13	
MPS A18	N	000	000	00	0000	13	
MPS A55	P	000	0000	0	00	13	
MPS A56	P	0000	0000	0	00	13	
MPS U01	N	00	00000	000	00	14	
MPS U05	N	000	00000	000	00	14	
MPS U56	P	00000	00000	000	00	14	
MPS2926	N	0	00	00	00	13	
MPS3394	N	00	00	00	000	13	
MPS3702	P	00	000	00	000	13	
MPS3706	N	0	0000	00	000	13	
MPS6514	N	00	00	0	0000	13	
TIP29	N	00	0000	0000	0	3	
TIP30	P	00	0000	0000	0	3	
TIP31	N	00	00000	00000	0	3	
TIP32	P	00	00000	00000	0	3	
TIP140	N	000	00000	00000	0000	7	Darlington
TIP142	N	00000	00000	00000	0000	7	Darlington
TIP2955	P	000	00000	00000	0	3	
TIP3055	N	000	00000	00000	0	3	
TIP5530	P	000	00000	00000	0	3	
2N696	N	000	0000	00	0	2	
2N705	N	0	0	00	0	2	
2N914	N	0	0000	00	00	2	
2N1613	N	000	0000	00	00	2	
2N1711	N	000	0000	00	000	2	
2N1983	N	00	0000	00	000	2	
2N1984	N	00	0000	00	000	2	
2N2219	N	00	0000	00	00	2	
2N2222	N	00	0000	00	00	2	
2N2925	N	00	00	0	0000	13	
2N2955	P	00	00	0	0	2	
2N3054	N	000	00000	00000	00	7	
2N3055	N	000	00000	00000	0	7	
2N3553	N	00	0000	00	000	2	
2N3568	N	000	0000	0	000	13	
2N3638	P	00	0000	0	000	13	
2N3702	P	00	0000	0	000	13	
2N3666	N	00	0000	000	0	2	
2N3904	N	00	000	00	00	13	
2N3905	P	00	000	00	000	13	
2N3906	P	00	000	00	000	13	
2N3907	N	000	00	00	000	13	
2N4123	N	00	000	0	00	13	
2N4124	N	00	000	0	00	13	
2N4126	P	00	000	0	000	13	
2N4401	N	00	0000	00	0	13	
2N4410	N	0000	0000	00	000	13	
2N4427	N	0	0000	000	0	2	
2N5183	N	0	0000	000	000	2	

①



②



③



④



⑤



⑥



⑦



⑧



⑨



⑩



⑪



⑫



⑬



⑭

grounded base: f_T = 700 MHz

low noise

grounded base: f_T = 675 MHz
 grounded base: f_T = 220 MHz
 grounded emitter: f_T = 260 MHz
 grounded emitter: f_T = 200 MHz
 grounded emitter: f_T = 550 MHz
 grounded base: f_T = 240 MHz
 grounded emitter: f_T = 260 MHz
 grounded emitter: f_T = 50 MHz
 grounded emitter: f_T = 260 MHz
 f_T = 70 MHz
 grounded emitter: f_T = 1000 MHz
 grounded emitter: f_T = 1000 MHz

f_T = 150 MHz
f_T = 200 MHz
f_T = 750 MHzf_T = 300 MHzf_T = 100 MHzf_T = 480 MHz

≠ MJE2955, TIP2955!

f_T = 500 MHzf_T = 700 MHzf_T = 700 MHz

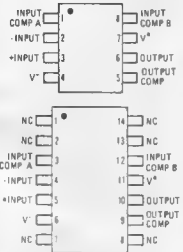
OPAMPS, COMPARATORS

703



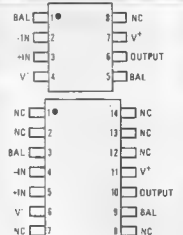
NOTE: Pin 4 connected to case.

709

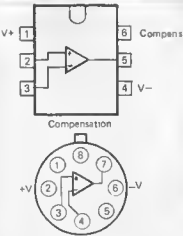


NOTE: Pin 7 connected to bottom of package.

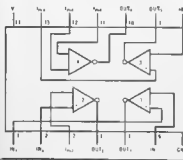
741 (835, 844)



TAA 861 (A)



LM3900

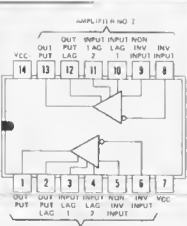


NOTE: All IC's shown top view, unless otherwise stated.

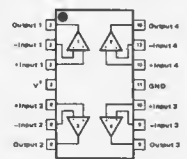
1458 (5566)



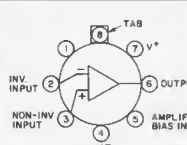
SN 76131 = TRA 231 = LA 739



324

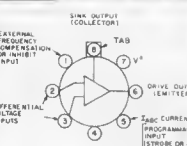


CA 3080

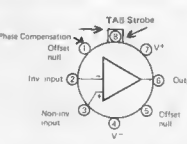


NOTE: Pin 4 is connected to case.

CA 3094

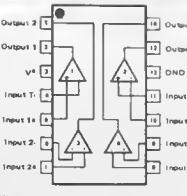


CA 3130



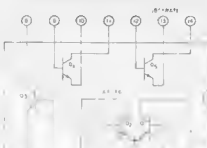
NOTE: Pin 4 is connected to case.

339 (3302)



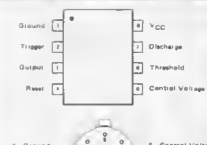
SPECIAL TYPES

CA 3086 = CA 3046

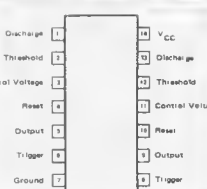


BOTTOM VIEW

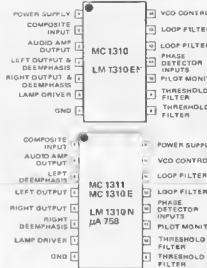
555



556

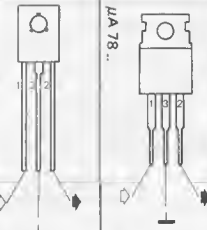


1310

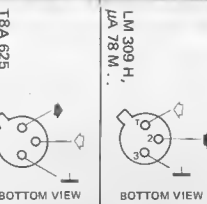


VOLTAGE REGULATORS

L 129/L 130/L 131



T8A 625 (829, 830)



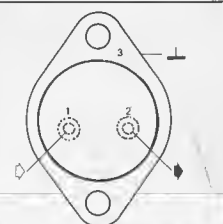
BOTTOM VIEW

LM 309 H, JA 78 M.

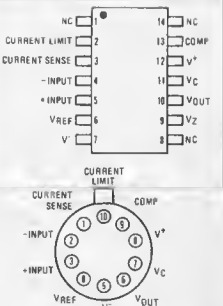


BOTTOM VIEW

LM309K

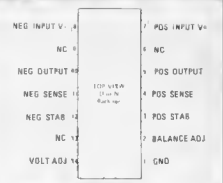


723 (550)

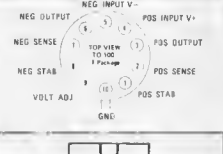


NOTE: On metal can, pin 5 is connected to case.

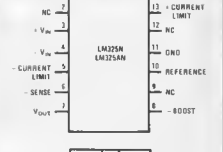
SG 3501 (SG 4501)



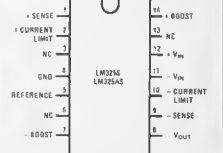
LM 325 (LM 125/LM 225)



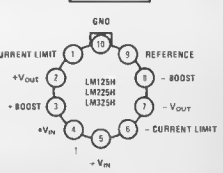
LM 325 (LM 125/LM 225)

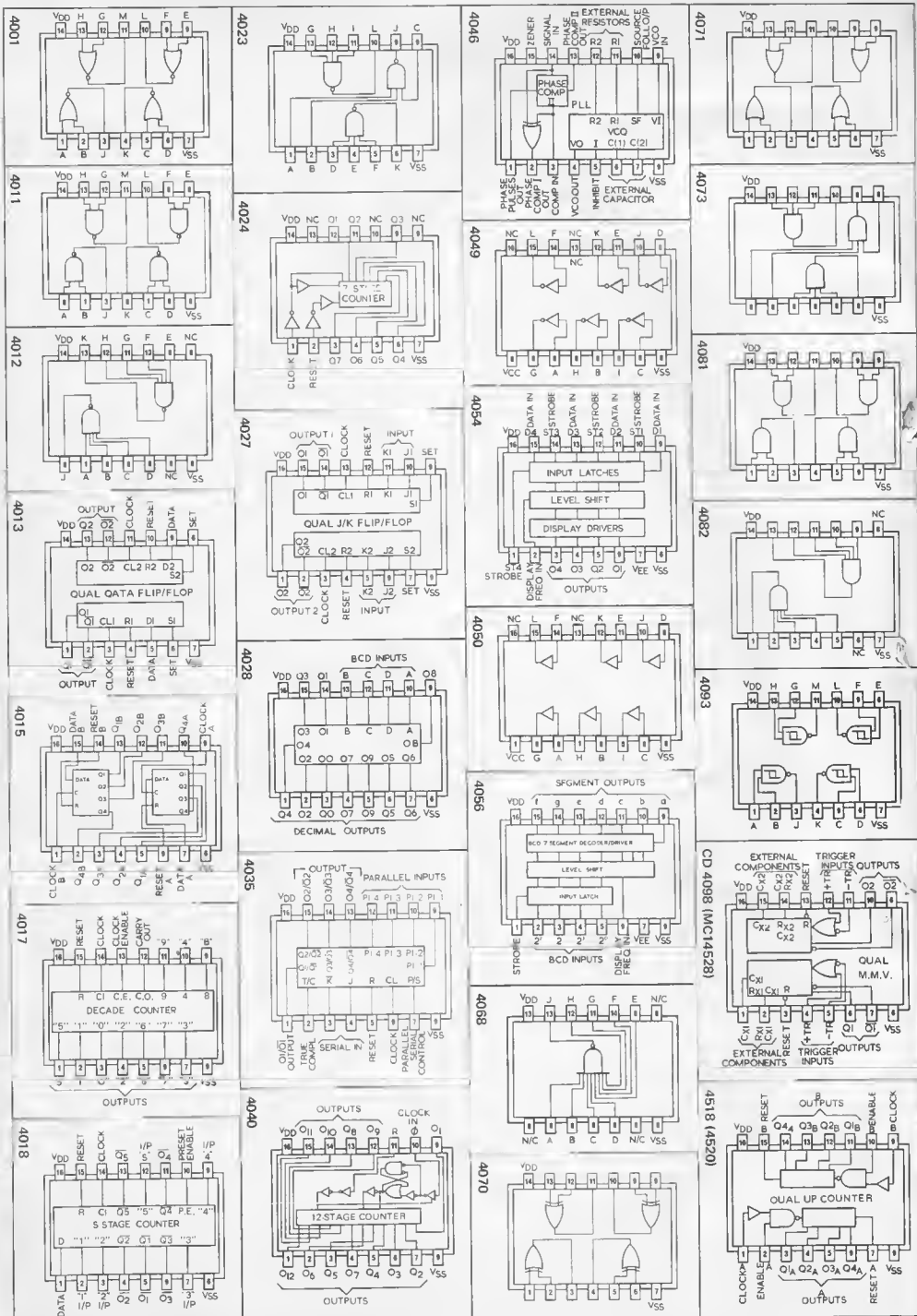


LM 325 (LM 125/LM 225)

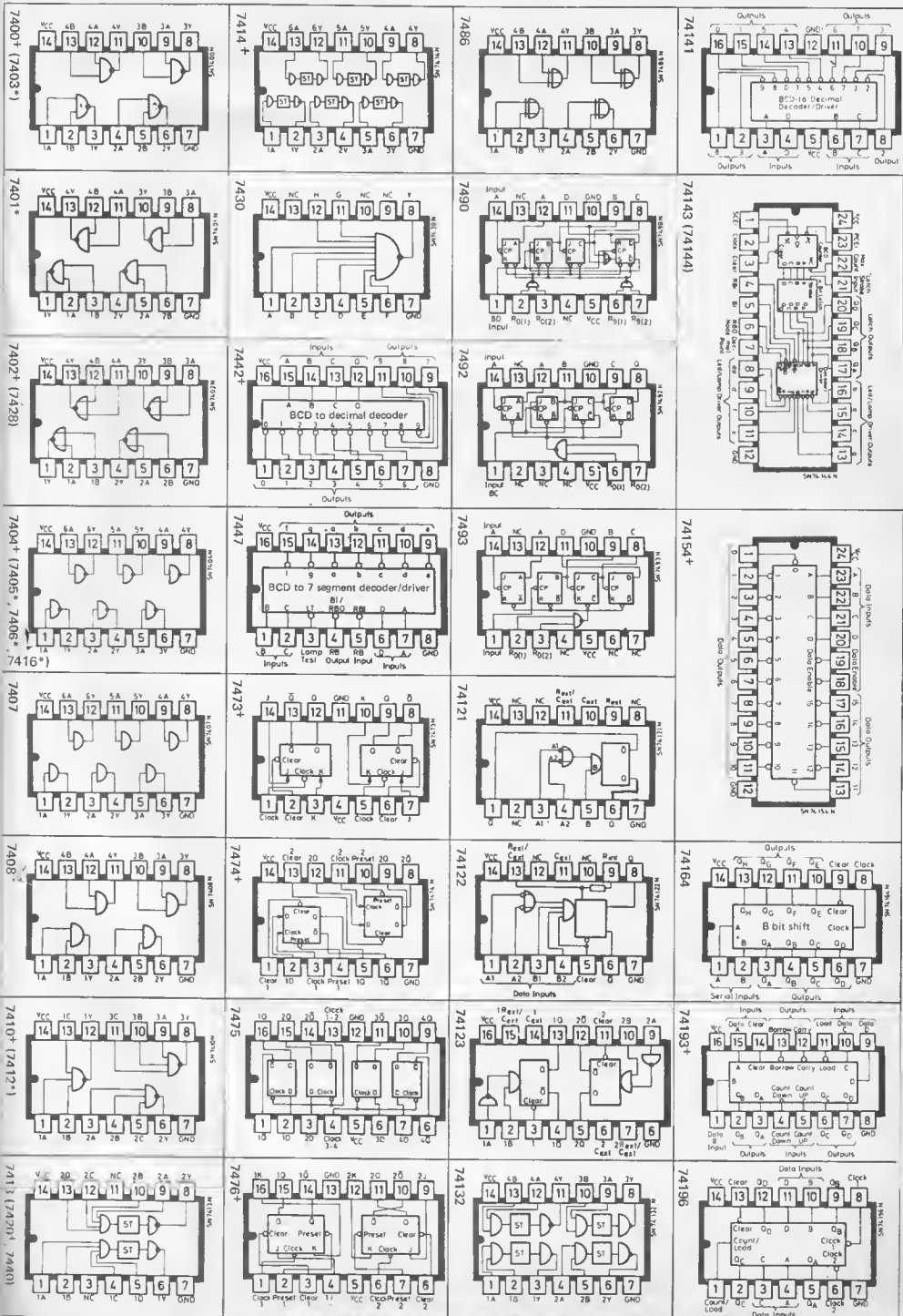


LM 325 (LM 125/LM 225)





Note: A prefix to the type number denotes the manufacturer, e.g. CD 4001 (RCA), MC 14001 (Motorola), N 4001 (Signetics), SCL 4001 (Solid State Scientific), SIL 4001 (Siiteck).



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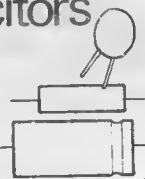


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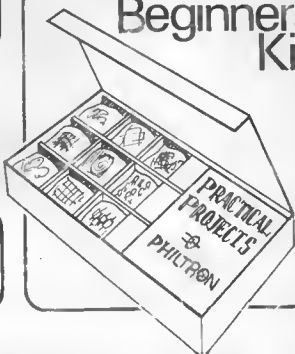
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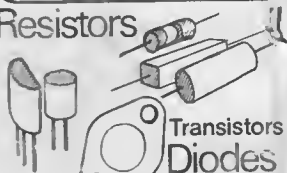
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